A Simulation Example of SAMOC

With the device models presented in chapter 2 and the simulation techniques presented in chapter 3, SAMOC can analyze DC solutions of MOS circuits. In order to test the models and the simulation techniques, some simple circuits are selected to be analyzed by SAMOC.

One of the most important circuit parts in analog CMOS circuit design is the differential amplifier. A differential amplifier is usually used in comparing two voltage signals. Typically, a differential amplifier has two inputs and its output is a function of the difference of two inputs. Most of time, the output gain is designed to be large to emphasize the difference of two inputs.

One of the best differential amplifiers that can work well inside the allowed range is the wide-range transconductance amplifier presented in [mead]. The schematic of the wide-range transconductance amplifier which is constructed by 4 PMOS and 5 NMOS transistors, is shown in Fig. 1.

By adding some extra code, it is possible to monitor the state change details while SAMOC is finding out the DC solution of a circuit. Table 1 shows the state changing detail of 9 MOS transistors in the wide-range transconductance amplifier shown in Fig. 1 with V+ = 1.05V and V- = 1.00V.

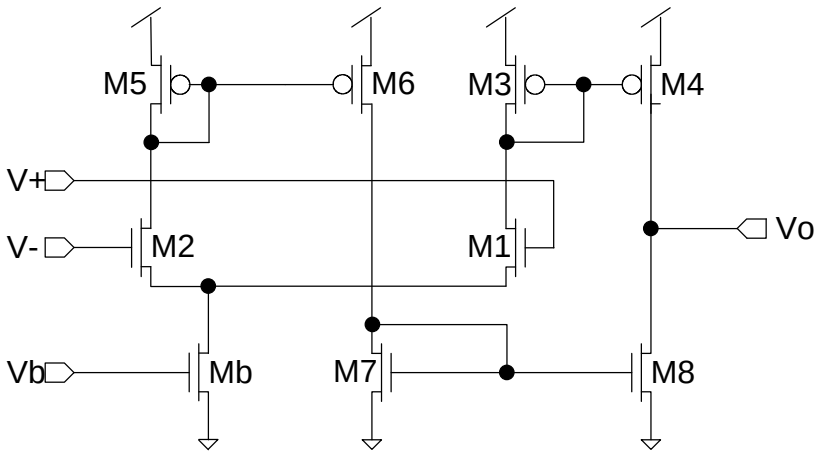

Fig. 1 Schematic of the wide-range transconductance amplifier.

The first column of the Table 1 is the iteration index. SAMOC solution seeking algorithm found out that the solution in 7th and 8th steps confirm the convergence of the algorithm. At the first step, all MOS transistors were set to be in state 1 (cutoff region). Step 2 is the preset region and each MOS transistor's state was directly set by the terminal voltages calculated by the states set by step 1. After step 2, Katzenelson algorithm is applied. From step 2 to step 1, the minimum scaling factor t_{min} limit the state changes. Most of time, only one MOS transistor is allowed to change its state at each iteration step. Sometimes, if two MOS transistors have identical gate and drain, then these two MOS transistors can change states at the same time. Table 1 shows from step 2 to 3, M7 and M8 change states at the same step. After step 3, only

one MOS transistor changes working region (state) at each iteration step. Fig. 2 shows the change of the output voltage (Vo) during the solution seeking procedure of SAMOC. Note that there is no state change from step 7 to 8 in Table 1 and there is no numerical value change in the plot presented in Fig. 3, either. Vo is low and according to V+ =1.05V and V- =1.00V, the answer is acceptable.

	M5	M6	M3	M4	M2	Mb	M7	M1	M8	remarks
1	1	1	1	1	1	1	1	1	1	initial guess
2	2	2	2	2	1	2	1	1	1	preset
3	2	2	2	2	1	2	2	1	2	M7, M8 changed
4	2	2	2	2	1	3	2	1	2	Mb changed
5	2	2	2	2	2	3	2	1	2	M2 changed
6	2	2	2	2	2	3	2	1	3	M8 changed
7	2	2	2	2	2	3	2	2	3	M1 changed
8	2	2	2	2	2	3	2	2	3	no change, **f** is small, iteration stops

Table 1 State transition table

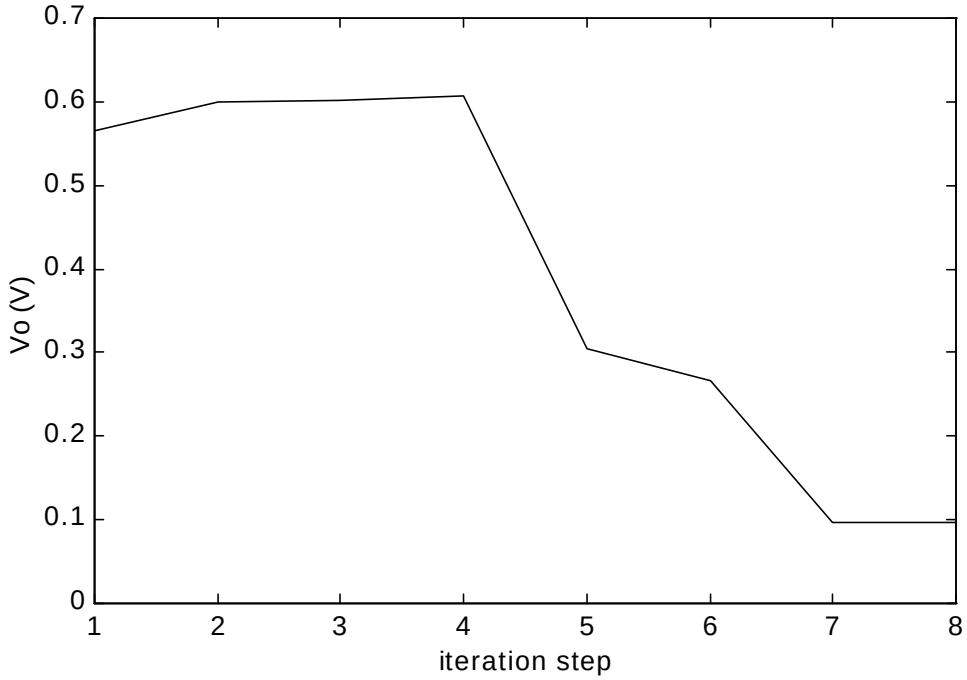

Fig. 2 The output voltage as a function of iteration step index.

Comparison with SPICE Simulation via DC Sweep

Fig 2 shows an likely acceptable result of the SAMOC simulation. One question may be asked at this point: "How much similar the result is to the SPICE simulation?" This section presents and compares the functional analyses of SAMOC and SPICE simulations. The best way to compare the DC analyses is to do the linear DC sweep of a circuit by both SAMOC and SPICE simulators. The analyzed circuit is still the wide-range transconductance amplifier illustrated in Fig. 1. The DC sweep analyses were performed 5 times with V- =0.5V, 1.5V, 2.5V, 3.5V and 4.5V respectively and V+ values are swept from 0V to 5V. The SPICE simulation was performed by PSPICE® version 8.0 of MicroSim®. Both SAMOC and PSPICE were running on the same computer with MicroSoft® Windows95® operating system, 64 Megabytes of SDRAM and a Cyrix® 6x86MX® PR200 CPU.

Fig. 3 shows the PSPICE DC sweep results obtained by using level-3 model. All PMOS transistors have device geometry specified by w = 6u and l = 2u. All NMOS transistors have w = 2u and l = 2u. The values marked on the lines are the values of V-.

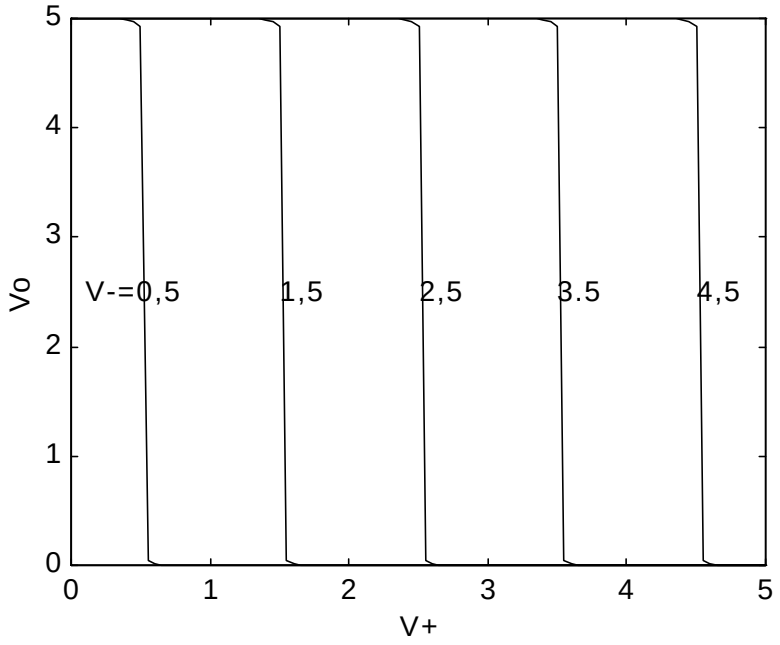

Fig. 3 PSPICE DC sweep

Fig. 4 shows the DC sweep analyses obtained by SAMOC simulation. Since the sophisticated DC sweep algorithm has not yet been built in SAMOC, for functional verification, SAMOC calls the same DC analysis subroutine and changes the V+ values to record the result. Fig. 3.7 shows that the DC sweep results approach the SPICE results. The big difference happens when V- =0.5V and V+ is smaller than 0.7V. The difference may be caused by the SAMOC MOS models does not take subthreshold behavior into account.

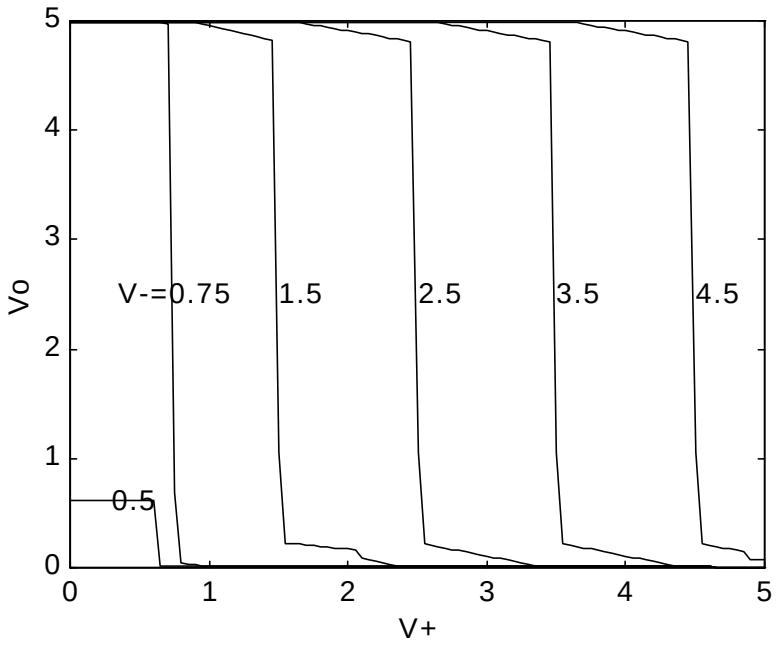

Fig. 4 SAMOC DC sweep