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Compact Tunable Current-Mode Analog Circuits Using DGMOSFETs

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Introduction

Double-Gate (DG) MOSFET has vast potential in analog circuit applications as a four-terminal device, where the top-gate response may be conveniently tuned via bottom gate bias [1,2]. This has a number of important implications for circuit design: i) increased functionality out of a given set of devices; ii) reduction of device layout area and parasitics; and iii) higher-speed operation and low-power consumption with respect to equivalent conventional circuits. Despite such advantages, however, analog applications of DG-MOSFETs have not received the due attention compared to digital reconfigurable systems [3,4]. In the present work we address this issue and show how compact low-power analog circuits may be built using DG-MOSFETs together with current-mode design techniques.

In low-power analog systems, current-mode signal processing has been usually considered an attractive strategy due to its potential for high-speed operation and low-voltage compatibility [3,5]. The current-mode circuits are especially suitable for DG-MOSFETs optimized for low-voltage operation. Tunable current-mode circuit blocks investigated here using TCAD simulations include a current mirror, a differential current amplifier and an integrator. Therefore, our work provides valuable insight into novel current-mode analog design strategies and circuits based on DG-MOSFETs normally optimized for digital applications.

DGMOSFET Structure and Modeling

DG-MOSFETs considered in this study are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with minimal overhead to the fabrication sequence. This implies using DG-MOSFETs with a minimal body thickness ($t_{Si}\leq$30nm), oxide insulator thickness ($t_{ox}\leq$5nm) and gate length (L$\leq$100nm), and maximum I_{ON}/I_{OFF} ratio optimized normally for minimum switching delay•power product [6]. It is also assumed that both gates have been optimized for symmetrical threshold $V_T=\pm$0.25V using a dual-metal process. A generic DG-MOSFET structure based on these design guidelines and in agreement with the experimentally demonstrated devices is given in Fig.1. 2D simulations of this structure are accomplished using DESSIS [7] in drift-diffusion approximation for carrier transport, which is sufficient for low-power circuit-configurations explored here. Fig.1 shows a typical current-density distribution in an asymmetrically biased n-type DG-MOSFET, where the higher bias of top-gate induces a more conductive channel.

With the device structure fixed, we can tailor analog performance by the use of bottom-gate bias. This is best illustrated in Fig.2, where the drain current through *n*- type DG-MOSFETs driven from top-gate is studied as a function of bottom gate bias. While the threshold of individual DG-MOSFETs can be modified using this approach, it must be pointed out that the resulting independently driven devices (IDDG, Fig.3a) are always inferior to symmetrically driven counterparts (SDDG) in terms of transconductance and sub-threshold performance, under equal geometry and bias conditions [1]. Thus bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by variety of circuit possibilities, as explored below.

Tunable Current Mirrors

The simple tunable DG current mirror (see Fig.3b) constitutes one of the most important analog circuit blocks [8]. Fig. 4 shows that for a given input current we can get different output current values depending on the setting voltage (Vseto). The required voltage across the input device for DG current mirror is less than that required for conventional MOS current mirror (Fig.5). Fig.6 shows the relation between output current and setting voltage (Vseto) for different Vref values used to set input current I_{IN}. As shown from the simulation results the DG current mirror has major advantages over conventional MOS current mirror such as lower voltage supply and power dissipation (lower V_{IN}) and ii) tunability without the use of an extra transistor (less area and parasitics).

Current-Mode Tunable Circuits

In the case of a DG differential current amplifier (see Fig.3c) it is possible to achieve appreciable gain and bandwidth programming using various biasing schemes for the back-gate control voltages on the input and output sides (Vseti, Vseto), as shown in Fig. 7 and Fig.8. By combining biasing schemes in Fig.7 and Fig.8, it should be possible to tune both gain and bandwidth in a single stage. Once again, this is achieved without the use of extra transistors found in conventional CMOS circuits, thus reducing area, supply and power requirements considerably. A unique advantage of current-mode circuits is the elimination of gain-bandwidth trade-off that besets signal processing in voltage domain. This is vividly illustrated in DG differential current integrator in Fig.9, but also found in Fig.7 & Fig.8. The integrator in Fig.9 is a modified version of circuit proposed in [9,10], albeit using only 8 transistors (down from 12).

[1] M V R Reddy et al., IEEE Elec Dev. Lett., 26, pp.664, 2005.
[2] L. Mathew et al., Proc. IEEE SOI Conference, pp.187, 2004.
[3] S Kaya et al., 6th IEEE Conf. Nanotech, July 16-20, 2006. Cincinnati.
[4] P Beckett, GLSVLSI'03, April 28-29, 2003, Washington, DC.
[5] J. A. De Lima, Analog Int. Circ. & Sig. Proc., 41, pp.147, 2004.
[6] C-H Lin et al., Proc. ISDRS,pp.266,2003.
[7] ISE TCAD Suite, http://www.synopsis.com.
[8] A. Kumar and S Tiwari, Proc. of ISCAS, vol.I, pp.197, 2004.
[9] S. L. Smith and E. Sánchez-Sinencio, IEEE Trans. on Circ. and Syst.-II, Vol. 43, pp. 39-48, 1996.
[10] X. Quan, et al., Elec. Lett., vol. 34, pp.1-2, 1998.

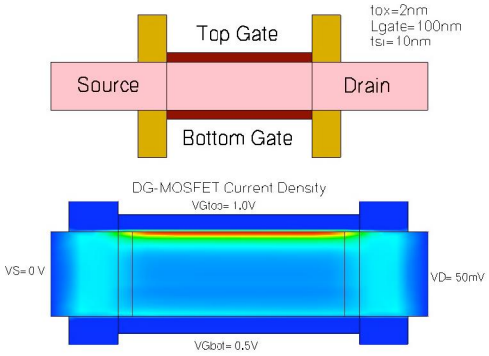

FIGURE 1: The DG-MOSFET device structure (top) used in this work has a gate length L_g=100nm, t_{Si}=10nm and t_{ox}=2nm, typical values for digital applications. Current density distribution at an asymmetric bias condition is shown above, with the top channel fully on and bottom channel is weaker.

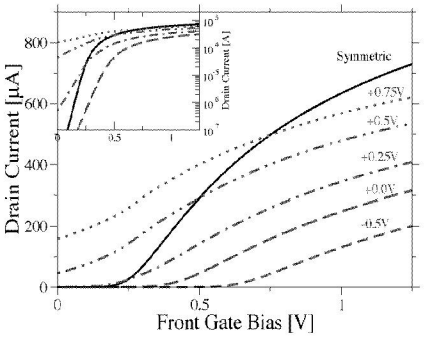

FIGURE 2: Simulated I_D-V_{Gtop} plots of DG-MOSFET at different back gate bias conditions and symmetric (V_{bg}=V_{fg}) drive condition. The inset shows deterioration of subthreshold slope of asymmetrically driven DG-MOSFETs, a well-known phenomenon tolerable in analog design.

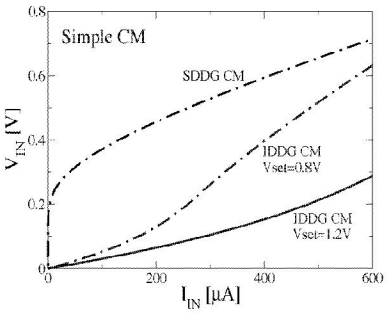

FIGURE 5: Comparison of the required voltage across the input transistor of the simple DG current mirror in three configurations: SDDG (conventional: no back gate control) and IDDG with two different bias voltages. Higher the back gate bias lower the input supply needed.

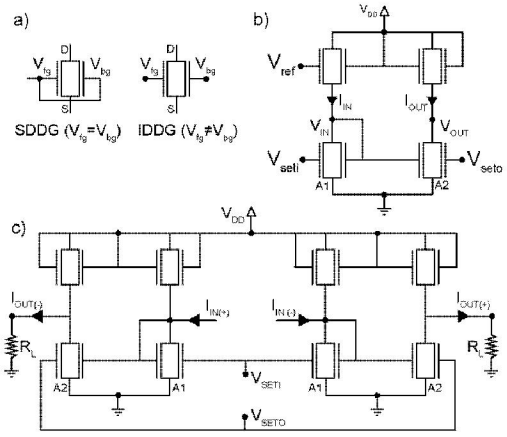

FIGURE 3: a) DG bias conventions SDDG and IDDG refers to *symmetrically* and *independently* driven dual-gates, respectively. b) a simple DG current mirror, and c) DG differential current amplifier used in this study. Back gates are used for control.

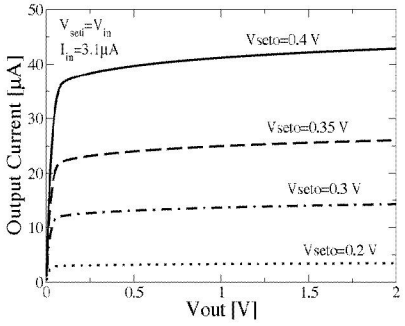

FIGURE 4: Simulated output current of a simple current mirror as a function of output voltage for various back-gate voltage (Vseto) of output transistor at a given input current bias of 3.1uA.

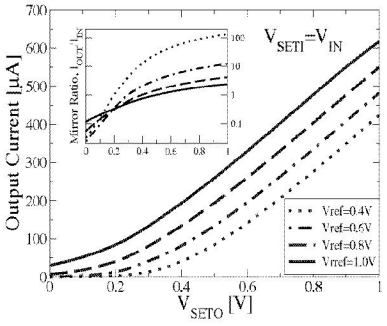

FIGURE 6: Output current for different reference voltage Vref (e.g. I_{IN}) vs output setting -voltage (Vseto). The inset shows the mirror ration between the output and input stage of the mirror.

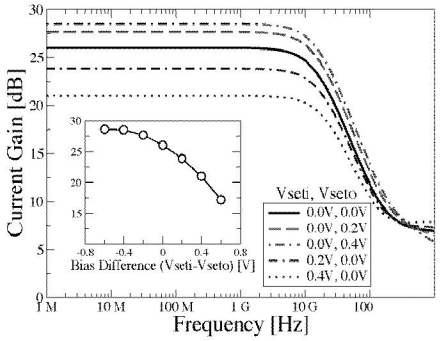

FIGURE 7: Gain vs. frequency response of the differential current amplifier for various setting voltage pairs (Vseti≠Vseto). The inset plots the extracted tuning curve for the amplifier. The case for Vseti=Vseto=0.0V is also given for comparison

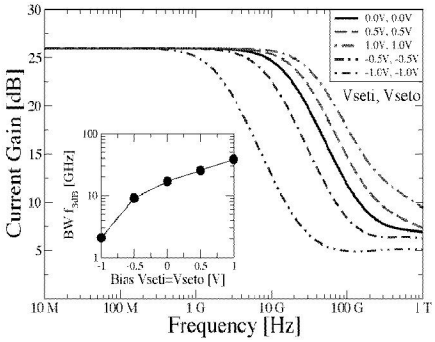

FIGURE 8: Gain vs. frequency response of the differential current amplifier for equal setting voltages (Vseti=Vseto). The inset plots the simulated tuning window for the bandwidth (BW, f_{3dB}) of the amplifier. Note that the BW may be tuned without change in the gain.

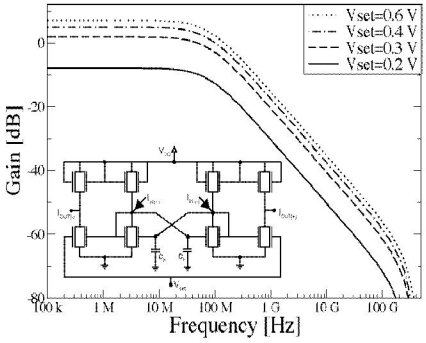

FIGURE 9: Gain vs. frequency response of the differential current integrator, built using two current mirrors in cross-feedback (inset), for different setting voltage (Vset). Clearly, the current-mode integrator, like the amplifier, evades the gain-BW trade-off.