NODAL APPROACH TO MULTIPLE-FAULT LOCATION IN ANALOG CIRCUITS

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ABSTRACT

The multiple-fault location problem for analog circuits is treated on the basis of the nodal equations. The availability of voltage measurements due to current excitations is assumed by the method. Topological restrictions on the possibility of fault location for a given set of measurements are formulated. The emphasis in this paper is on locating subnetworks or regions containing all the faults of the network. Coates flow-graph representation of a network is used for topological considerations.

INTRODUCTION

Testing of analog circuits with the aim of fault location is important in network analysis. There are different approaches to the problem depending on the information available from tests conducted on the network. Generally, the network topology is known and we try to identify the faulty elements and evaluate them. If the number of measurements is large enough we can evaluate all elements and single out the faulty ones [1,2]. However, when the number of measurements is limited we can use various methods to predict regions where faults may appear [3,4]. To verify whether a predicted region contains all the faults, the multiple-fault location method based on the multiport description of a network can be used [5].

In this paper, we present a method based on the nodal equations. Topological restrictions on multiple-fault location are discussed and it is shown how they may be effectively used to locate faulty regions. Some practical remarks for effective calculations are given.

MULTIPLE-FAULT VERIFICATION BY NODAL EQUATIONS

In this section we discuss the method of multiple fault location on the basis of the nodal equations. The principal difference between the nodal and the multiport approach is that in the multiport approach we aim to find changes in element values whereas in the nodal method we design the changes in nodal currents only. Changes in element values can be computed by the nodal method after the network topology is considered.

Nodal Equations for Faulty Network

Let us assume that the network has n+1 nodes, m of them accessible, and f < m is the number of faulty elements. The nodal equations for the nominal values of the elements have the form

$$Y V = J. \tag{1}$$

For the faulty network, assuming the same excitations, we obtain

$$(Y + \Delta Y)(V + \Delta V) = J. \tag{2}$$

Thus

$$Y \Delta V = -\Delta Y V', \qquad (3)$$

where $V' = V + \Delta V$ is the vector of nodal voltages in the faulty network. We can compute ΔV assuming that Y is nonsingular and obtain

$$\Delta y = - y^{-1} \Delta y y'. \tag{4}$$

Let us denote $\Delta J = -\Delta Y V'$. ΔJ represents changes in nodal currents caused by faulty elements. The relation (4) becomes

$$\Delta y = y^{-1} \Delta J. \tag{5}$$

We can assume that a few elements are faulty, in which case $\Delta\underline{J}$ has the form

$$\Delta \tilde{J} = \begin{bmatrix} \tilde{Q} \\ \Delta \tilde{J}^{F} \\ \tilde{Q} \end{bmatrix}. \tag{6}$$

Assuming that the first ${\tt m}$ nodal voltages can be measured we obtain

$$\begin{bmatrix} \Delta \underline{v}^{\mathsf{M}} \\ \Delta \underline{v}^{\mathsf{N}-\mathsf{M}} \end{bmatrix} = \underline{v}^{-1} \quad \begin{bmatrix} \underline{0} \\ \Delta \underline{J}^{\mathsf{F}} \\ \underline{0} \end{bmatrix} , \qquad (7)$$

where N indicates the set of all nodes and M the set of measurement nodes. Hence, $\,$

$$\Delta \underline{v}^{M} = \underline{z}_{MF} \Delta \underline{J}^{F}, \qquad (8)$$

where

$$\underline{\mathbf{Y}}^{-1} = \begin{bmatrix} \mathbf{Z}_{MN} \\ \mathbf{Z}_{N-M,N} \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{M1} & \mathbf{Z}_{MF} & \mathbf{Z}_{M2} \\ \mathbf{Z}_{N-M,1} & \mathbf{Z}_{N-M,F} & \mathbf{Z}_{N-M,2} \end{bmatrix}. \tag{9}$$

Relation (8) has to be satisfied when the set F of network nodes includes all nodes associated with

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Reduction of the Number of Equations

It is clear from relation (8) that in order to design ΔJ^F we must have at least 1 + card F measurement nodes. If there is an isolated fault in the network it causes changes in two elements of the ΔJ^F vector. In the example shown in Fig. 1 we have $\Delta J^F_k = -\Delta Y_e U^1 = -\Delta J^F_j$. In such a case vector

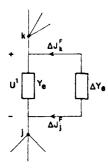


Fig. 1 Changes in nodal current caused by a single fault.

 ΔJ^F will contain variables which are not independent. We can transform the equation (8) to reduce the column rank of the coefficient matrix Z_{MF} . The reduction realized depends on the location of different faults. Let us discuss the following two cases.

- 1. If an isolated fault appears between nodes k and j (see Fig. 1) then equation (8) can be modified. We may replace column k of matrix $\underbrace{Z_{MF}}_{column}$ by the difference of columns k and j and remove column j as well as the jth component of vector $\Delta\underline{J}^r$.
- 2. If connected faults form a subtree $_F$ in the network then the number of variables in $\Delta \underline{J}^F$ can be reduced by one in similar way to Case 1. The reduction holds for every connected subgraph formed by faulty elements. If the subgraph contains a circuit then the number of variables can not be reduced.

TOPOLOGICAL RESTRICTIONS

A necessary conditions for solvability of equation (8) is full column rank of matrix Z_{MF} , which is equivalent to the existence of a square, nonsingular (card F) x (card F) submatrix of Z_{MF} .

Let Z_{EF} denote a square submatrix of Z_{MF} and Y (F¦E) denote the submatrix of Y obtained by removing F rows and E columns. Using the equivalence

$$\det Z_{EF} = 0 \iff \det X (F|E) = 0$$
 (10)

we can find topological restrictions for the fault location problem. Let us assume that the topological equations for the nodal admittance matrix and the Coates graph representation of the network are

$$\underline{Y} = \lambda \quad \underline{Y} \quad \lambda^{\mathrm{T}}. \tag{11}$$

where the element ij of λ is equal to 1 if the jth edge is directed towards the ith vertex, otherwise zero, and the element ij of λ is equal to 1 if the jth edge is directed away from the ith vertex, otherwise zero and \underline{Y}_e is a diagonal matrix of element admittances.

The submatrix $\underline{\Upsilon}$ (F¦E) can be presented in the form [6]

$$\underbrace{\mathbf{Y}}_{\mathbf{E}} (\mathbf{F}_{\mathbf{E}}) = \underbrace{\lambda}_{\mathbf{F}_{\mathbf{E}}} \underbrace{\mathbf{Y}}_{\mathbf{E}} \underbrace{\lambda}_{\mathbf{F}_{\mathbf{E}}}^{\mathbf{T}}, \tag{12}$$

where λ_{-F} (λ_{+E}) is obtained from λ_{-} (λ_{+}) by removing rows F (E), respectively.

Following Starzyk et al. [6] we can formulate the following theorem.

Theorem 1

If det \underline{Y} (F{E) \neq 0 then there exists at least one k-connection c_S in the graph G(F{E) obtained from the Coates graph of the network after deleting all the edges incoming to nodes F and all the edges outgoing from nodes E, where

$$S = \{(v_s, v_e); v_s \in Fn(N-E), v_e \in En(N-F)\},$$
 (13)

card
$$S = card (E n(N-F)) = card (F n(N-E)),$$
 (14)

(v_s, v_e) represents a path directed from the node v_s to the node v_e, and N is the set of all graph nodes \Box

The condition stated in Theorem 1 is sufficient almost everywhere. As a consequence of Theorem 1 we have an important corollary.

Corollary 1

If det \underline{Y} (F¦E) \ddagger 0 then after deleting all the edges outgoing from nodes E and incoming to nodes F there are no isolated nodes in the set N - (E \cap F) \square

To locate the faults of elements incident with nodes F such that after deleting all the edges incoming to nodes F some of them become isolated, we must include all of these isolated nodes in the set E, which means that all of them must be accessible nodes (i.e., the nodes at which voltages can be measured).

Let us investigate the problem of two subnetworks the graphs of which have a common nodes when a \leq card F. In this case we can not identify the faults appearing in one of the subnetworks by measuring the voltages in the second only because the k-connection required by Theorem 1 does not exist. But even in this case we still have the possibility of identifying the faulty region, where we check whether or not the only faults are included in a subgraph isolated from c+1 measurements by a c common nodes.

In the case when f faults appear in a subgraph connected to the rest of the graph through c common nodes, we must have at least f-c+1 measurements inside this subgraph to identify all these faults (see Fig. 2).

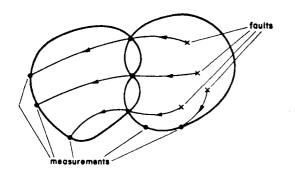


Fig. 2 Illustration of necessary measurements.

To ensure that the system of equations is overdetermined we should have at least two nonsingular (card F) x (card F) submatrices of Z_{MF} .

Lemma 1

If Z_{EF} is a nonsingular full column rank submatrix of Z_{MF} and z_{O}^{T} is a nonzero row of Z_{MF} not belonging to Z_{EF} then there exists a nonsingular submatrix of Z_{MF} that contains z_{O}^{T}

Proof

Since rank $Z_{MF} = \operatorname{rank} Z_{EF}$ the row z_0^T is a linear combination of rows $z_1^T \in Z_{EF}$, $i \in I$. If we remove row z_k^T , $k \in I$, then z_0^T will be linearly independent from the rows z_1^T , $i \in I - \{k\}$, and because of the linear independency of rows z_1^T will form a new set of linearly independent rows $\{z_0^T, z_1^T \in I, i \neq k\}$

Corollary 2

If Z_{MF} contains a zero row and the corresponding voltage $\Delta V^M \in \Delta V^M$ is nonzero then ΔJ^T does not represent all the faults in the network, therefore, other candidates for faults should be considered

To fulfill the condition stated in the Lemma 1 it is sufficient that there exists a node i ε M-E which is the origin of a path incoming to one of the F nodes, and if after deleting the edges incident to this path the remaining graph contains at least one 0-connection.

Element $z_{i,j} \in Z_{MF}$ is zero when there is no path directed from the node i to j or for every such path if I denotes the set of nodes belonging to the path det Y(I|I) = 0. The latter case is rare in electronic circuits.

SOME PRACTICAL REMARKS

Biernacki and Bandler [5] stated that condition (8) is satisfied if and only if the following relation holds

$$(\overline{Z}_{MF} - 1) \Delta \underline{V}^{M} = 0, \qquad (15)$$

where

$$\overline{Z}_{MF} \stackrel{\Delta}{=} Z_{MF} (Z_{MF}^{T} Z_{MF})^{-1} Z_{MF}^{T}. \tag{16}$$

Now we propose a simpler method which can be used to verify the condition (8).

One can prove that the solution of the equation

$$\overset{\mathbf{A}}{\mathbf{x}} \overset{\mathbf{x}}{=} \overset{\mathbf{b}}{\mathbf{b}},$$
 (17)

where \underline{A} is an mxf full column rank matrix f < m, exists if and only if it can be transformed to the form

after row manipulation, where b_1 is a column vector having f elements. The form (18) is also more convenient for obtaining the solution of the set of equations.

For ill-conditioned systems the method of Householder orthogonal transformations can be used to reduce to zero the subdiagonal elements of ${\mbox{\cite{A}}}$ [7].

For practical situations when both measurement errors and effects of tolerances appear, the technique proposed by Bandler, Biernacki and Salama [8] can be used. In the first stage of computation we solve an optimization problem that can be stated

minimize
$$\sum_{i=1}^{n} (|\text{Re}(\Delta J_{i}^{F})| + |\text{Im}(\Delta J_{i}^{F})|)$$
 (19)

subject to linear equality constraints (8). Solution of this problem gives us the most likely faulty elements. Then the verification technique in the presence of tolerances can be used to check (8) in the way described in [8].

Example

Consider the active lowpass filler having structure shown in Fig. 3. Measurements have been taken at nodes 10, 12, 15 and 17. We decompose the graph of the network into three subgraphs as shown in Fig. 4. We may check the necessary condition (8) for the subnetwork which contains all the measurements and find it to be fault free. In this case the set $F=\{10,15,17\}$ represents all the faulty nodes that can appear within incident subnetworks.

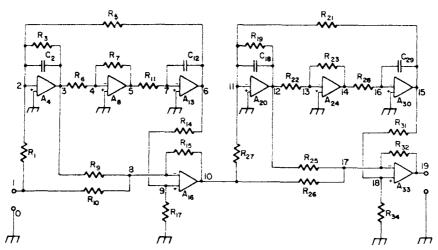


Fig. 3 Active lowpass filter example.

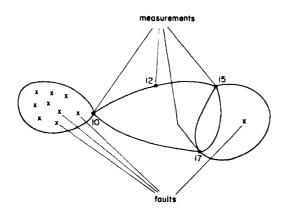


Fig. 4 Decomposition of the graph of the active filter into subgraphs.

CONCLUSIONS

The method presented extends the possibilities of multiport methods for multiple-fault location. Topological restrictions discussed in the paper show that in some cases faults cannot be identified if the measurements are imposed in the wrong place. Multiple-fault location analysis is necessary when we want to isolate faults inside a subnetwork without a sufficient number of measurements to identify all subnetwork components.

These topological restrictions can be effectively used when we investigate a subnetwork instead of the whole network. All the faults outside the investigated subnetwork can be appropriately respresented by assuming as faulty only the common nodes. This network partitioning into faulty or nonfaulty regions will be useful in fault analysis of large networks.

The authors believe that their approach together with the practical remarks presented permits more opportunities for effectively solving fault location problems in linear networks.

REFERENCES

- [1] T.N. Trick, W. Mayeda and A.A. Sakla, "Calculation of parameter values from node voltage measurements", IEEE Trans. Circuits and Systems, vol. CAS-26, 1979, pp. 466-474.
- [2] N. Navid and A.N. Wilson, Jr., "A theory and an algorithm for analog circuit fault diagnosis", <u>IEEE Trans. Circuits and Systems</u>, vol. CAS-26, 1979, pp. 440-457.
- [3] H.M. Merrill, "Failure diagnosis using quadratic programming", IEEE Trans.

 Reliability, vol. R-22, 1973, pp. 207-213.
- [4] M.N. Ransom and R. Saeks, "Fault isolation with insufficient measurements", <u>IEEE Trans.</u> <u>Circuit Theory</u>, vol. CT-20, 1973, pp. 416-417.
- [5] R.M. Biernacki and J.W. Bandler, "Multiple-fault location of analog circuits", IEEE Trans. Circuits and Systems, vol. CAS-28, 1981, pp. 361-367.
- [6] J.A. Starzyk, R.M. Biernacki and J.W. Bandler, "Design of tests for parameter identification by voltage measurements", Faculty of Engineering, McMaster University, Hamilton, Canada, Report SOC-266, 1981.
- [7] J.K. Reid, Ed., Large Sparse Sets of Linear Equations. New York: Academic Press, 1971.
- [8] J.W. Bandler, R.M. Biernacki and A.E. Salama, "A linear programming approach to fault location in analog circuits", Proc. IEEE Int. Symp. Circuits and Systems (Chicago, IL, 1981), pp. 256-260.