LOCATING STUCK FAULTS IN ANALOG CIRCUITS

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ABSTRACT

A new approach is proposed in this paper to detect the stuck faults in linear analog circuits. Ideal switches are inserted to indicate stuck-at, bridging and stuck-open locations. Then the resulting circuit is analyzed and stuck faults are directly identified. A recently developed method for multiple analog fault diagnosis is used eliminating a need for fault dictionary approach. The effect of locating stuck-at, bridging and stuck-open faults is modeled with full precision of resulting test conditions. An analog IC - μA741 is given as an example.

1. INTRODUCTION

Analog and mixed signal test and fault diagnosis have been among the most challenging topics in academic research and industrial exploration since the 1970s. Today, with the rapid development of applications using mixed signal products, this topic receives particular attentions from academia, design tool developers, ATE suppliers, designers and test engineers. This is demonstrated by a steady growth in the number of conference and journal papers, professional workshops and special journal issues related to this topic. Several periodical reviews for analog testing appeared in 1985 [1], 1991 [2] and 1998 [3].

Unlike its counterpart - digital test with efficient fault models and test methodologies - analog and mixed signal test and fault diagnosis is less advanced. This is mostly due to the inherited features such as parameter tolerances, poor controllability and limited accessible nodes. There is no widely accepted paradigm for analog and mixed signal test and fault diagnosis even with the introduction of IEEE 1149.4 Mixed-Signal Test Bus Standard. As expected, the research in analog and mixed signal test and fault diagnosis is strongly influenced by the advances in digital test. Design-for-Testability and Built-in-Self-Test in analog and mixed signal systems are two obvious examples that utilize the working paradigms of digital test. Another widely used paradigm of digital test is the stuck-at model combined with output logic level monitoring. In this model, it is assumed that all failure mechanisms manifest themselves as a single node stuck at logic 0 or 1. Based on this model, many digital test algorithms and techniques were developed [4].

Stuck-at, bridging, and stuck-open faults also happen in the analog designs, especially with today's increased complexity and increased die size of analog chips originated from different short, bridging or open failure mechanisms. The models of stuck-at, bridging and stuck-open faults have been reported in [3, 5] and their application in analog fault simulation, fault detection, and test generation can be found in [3, 6-7]. To test and diagnose these faults, the primary tactics of these fault-based approaches are to utilize dictionary approach through comprehensive simulation on the circuit with inserted fault model before test. Fault detection and location is determined by the comparison between measured signature and signature precompiled in the dictionary. Hence it requires many simulations and extensive fault dictionary. In this paper, a new method is proposed to locate the multiple stuck-at, bridging and stuck-open faults by verification approach without repetitive simulation needed for fault dictionary. An ideal open switch is inserted between the interested circuit nodes (bridging fault), or between the interested circuit node and the potential fault source – voltage source or ground. To model a stuck-open fault, a shorted switch is inserted in series with a line or a component. Simultaneously, such a serial switch together with an unknown-value admittance component can model the parametric faults. The constitutive equations of ideal switches derived from the KCL are combined with the other constitutive equations of the circuit parameters to construct the modified nodal equations for the newly resulting circuit. Note that the ideal switches do not exist physically in the circuits. A recently developed method for the multiple analog fault diagnosis is utilized to detect and locate all these faults exactly based on limited measurements of circuit responses [8-10].

2. APPLICATION OF STUCK-AT, BRIDGING AND STUCK-OPEN MODEL

Usually the topology of circuit under test (CUT) and its parameters' nominal values are known. Suppose that the CUT has $n+1$ nodes. Applying the KCL to each node of the CUT and all circuit parameters that do not have an admittance description such as inductors, current-controlled sources and operational amplifiers, we can obtain the modified nodal equation as follows [11]:

$$T_l X_l = W_l \tag{1}$$

where T_l is a lxl coefficient matrix, X_l is a $lx1$ vector of node voltage and parameter currents, and W_l is a $lx1$ excitation vector. Note that $l=n$ for normal nodal analysis of a circuit in which all parameters have admittance description, and $l>n$ for modified nodal analysis of a circuit in which some parameters have non-admittance description.

Assume that we are only interested in s potentially stuck-at faults in the CUT: ss of s are stuck-at and bridging faults and so of s are stuck-open faults($s=ss+so$). The ideal open switch SW_v $(v=1, 2, \ldots ss)$ is inserted between each pair of nodes i_v and j_v which has a potential for a bridging fault. Node i_v or j_v is connected to voltage source for stuck-at-1 fault, or ground for stuck-at-0 fault. Current I_v flows from node i_v to node j_v [Fig. 1.a]. For stuck-open fault, a shorted switch SW_v ($v=1, 2, \ldots, so$) is between i_v and a newly created node j_v.

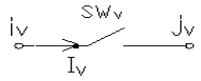

Figure 1.a model of ideal open switch

$$\begin{array}{c} \\ i_n \\ j_n \\ l+1 \end{array} \begin{array}{c} \begin{array}{ccc} i_n & j_n & l+1 \end{array} \\ \begin{bmatrix} & & 1 \\ & & -1 \\ F & -F & F-1 \end{bmatrix} \end{array}$$

Figure 1.b Modified coefficient matrix with an ideal switch

According to KCL, the constitutive equation to describe the ideal switch SW_v is as follows:

$$F(V_{i_v} - V_{j_v}) + (F-1)I_v = 0 \tag{2}$$

where variable *F* is 0 for the open switch and 1 for the closed switch [11]. Totally, *s* such equations are obtained.

Simultaneously, current I_v is added to KCL equation at node i_v while I_v is subtracted from KCL equation at the node j_v. Therefore, the coefficient matrix of modified nodal equations is augmented by one ideal switch SW_v [Fig. 1.b]. The resulted modified nodal equation with all *s* switches is as follows:

$$\begin{bmatrix} T_l & e_{i_1}-e_{j_1} & e_{i_2}-e_{j_2} \dots & e_{i_s}-e_{j_s} \\ F(e_{i_1}-e_{j_1})^T & & & \\ F(e_{i_2}-e_{j_2})^T & & (F-1)I_{sxs} & \\ \dots & & & \\ F(e_{i_s}-e_{j_s})^T & & & \end{bmatrix} \begin{bmatrix} X_l \\ I_1 \\ I_2 \\ \dots \\ I_s \end{bmatrix} = \begin{bmatrix} W_l \\ 0_{sx1} \end{bmatrix} \tag{3}$$

where superscript *T* represents the transpose of matrix or vector, I_{sxs} is a *sxs* unit matrix, 0_{sx1} is a *sx1* zero vector and e_i represents an *lx1* vector of zeros except for the i^{th} entry, which is equal to one.

Let us define an *lxs* matrix A which is to describe the locations of ideal switches in the circuit:

$$A = \lfloor e_{i_1}-e_{j_1} \;\; e_{i_2}-e_{j_2} \dots e_{i_s}-e_{j_s} \rfloor \tag{4}$$

Hence, the coefficient matrix in (3) has the following form

$$\begin{bmatrix} T_l & A \\ FA^T & (F-1)I_{sxs} \end{bmatrix} \tag{5}$$

For the fault-free circuit, all switches in the stuck-at and bridging models are open, i.e., *F=0*. For the faulty circuit, only switches corresponding to stuck-at and bridging faults are closed, i.e., *F=1*, while the rest are still open. This observation is reversed for the stuck-open models.

For simplicity, all switches in stuck-at and bridging models are separated with all switches in stuck-open models in the modified nodal equation (3), which can be implemented by matrix permutation. Hence, the matrix *A* is separated as

$$A = [A_{ss} \;\; A_{so}] \tag{4.a}$$

Applying (3) to fault-free circuit to obtain

$$T_0 X_0 = W_0 \tag{6}$$

where X_0 is an *(l+s)x1* solution vector, W_0 is an *(l+s)x1* excitation vector, and *(l+s)x(l+s)* coefficient matrix

$$T_0 = \begin{bmatrix} T_{l0} & A_{ss} & A_{so} \\ 0_{ssxl} & -I_{ssxss} & 0_{ssxso} \\ A_{so}^T & 0_{soxss} & 0_{soxso} \end{bmatrix} \tag{6.a}$$

Suppose that only *f* of *s* stuck faults really occurred in the faulty circuit. Among *f* faults, there are *fs* of *ss* stuck-at and bridging faults and *fo* of *so* stuck-open faults (*f=fs+fo*). Therefore, only *fs* of *ss* switches in stuck-at and bridging models are closed while the remaining *ss-fs* switches are still open. Similarly, *fo* of *so* switches in stuck-open models are open while the remaining *so-fo* switches are closed. Assume that excitations for the faulty circuit are the same as those of fault-free circuit, and all *f* switches are permuted for simplicity such that all *fs* and *fo* switches are ordered first among *ss* and *so* switches, respectively. The modified nodal equation for faulty circuit is:

$$TX = (T_0 + \Delta T)(X_0 + \Delta X) = W_0 \tag{7}$$

$$T = T_0 + \Delta T \tag{8}$$

$$X = X_0 + \Delta X \tag{9}$$

where

$$T = \left[\begin{array}{c|c|cc|c} T_{l0} & & A & & \\ A_{fs}^T & & 0_{fsxs} & & \\ \hline 0_{(ss-fs)xl} & 0_{(ss-fs)xfs} & -I_{(ss-fs)x(ss-fs)} & 0_{(ss-fs)xso} & \\ \hline 0_{foxl} & 0_{foxss} & -I_{foxfo} & 0_{fox(so-fo)} & \\ \hline [A_{so} \mid A_{fo}]^T & & 0_{(so-fo)xs} & & \end{array}\right] \tag{10}$$

$$A_f = \lfloor A_{fs} \;\; A_{fo} \rfloor = [e_{i_1}-e_{j_1}, e_{i_2}-e_{j_2}, ..., e_{i_{fs}}-e_{j_{fs}}, e_{i_{fs+1}}-e_{j_{fs+1}}, ...e_{i_f}-e_{j_f}] \tag{11}$$

$$\Delta T = \left[\begin{array}{c|c|cc|c} 0_{lxl} & & 0_{lxs} & & \\ A_{fs}^T & I_{fsxfs} & 0_{fsx(ss-fs)} & 0_{fsxso} & \\ \hline 0_{(ss-fs)xl} & & 0_{(ss-fs)xs} & & \\ \hline -A_{fo}^T & 0_{foxss} & -I_{foxfo} & 0_{fox(so-fo)} & \\ \hline 0_{(so-fo)xl} & & 0_{(so-fo)xs} & & \end{array}\right] \tag{12}$$

In (10), $[A_{so} \mid A_{fo}]$ denotes removing sub-matrix A_{fo} from the matrix A_{so}. Define two *(l+s)xf* matrices P_f and Q_f as follows:

$$P_f = \begin{bmatrix} 0_{lxf} \\ \hline I_{fsxfs} \mid 0_{fsxfo} \\ 0_{(ss-fs)xf} \\ \hline 0_{foxfs} \mid I_{foxfo} \\ 0_{(so-fo)xfs} \end{bmatrix} \tag{13} \qquad Q_f = \left[\begin{array}{c|c} A_{fs} & -A_{fo} \\ \hline I_{fsxfs} & 0_{fsxfo} \\ \hline 0_{(ss-fs)xf} & \\ \hline 0_{foxfs} & -I_{foxfo} \\ \hline 0_{(so-fo)xf} & \end{array}\right] \tag{14}$$

then ΔT is the matrix product of P_f and Q_f^T:

$$\Delta T = P_f Q_f^T \tag{15}$$

and (7) can be re-written as

$$(T_0 + P_f Q_f^T)(X_0 + \Delta X) = W_0 \tag{16}$$

After substituting (6) into (16), ΔX can be solved by

$$\Delta X = -T_0^{-1} P_f \; Q_f^T X \tag{17}$$

Denote an $(l+s)x(l+s)$ matrix S_0 as follows

$$S_0 = [s_1 \; s_2 \; \ldots \; s_{l+s}] = -T_0^{-1} \tag{18}$$

and rewrite vector X in scalar form:

$$X = [x_1 \; x_2 \; \ldots \; x_l \; I_1 \; I_2 \ldots I_s]^T \tag{19}$$

where $s_v \; (v = 1, 2, \ldots, l+s)$ is an $(l+s)x1$ vector while $x_v \; (v = 1, 2, \ldots, l)$ and $I_v \; (v = 1, 2, \ldots, s)$ are numbers.

Denote the matrix product of S_0 and P_f as S_F, and product of Q_f^T and X as l_F:

$$\begin{aligned} S_F &= S_0 P_f = [s_{l+1} \; s_{l+2} \ldots s_{l+fs} \; s_{l+ss+1} \; s_{l+ss+2} \ldots \; s_{l+ss+fo}] \\ l_F &= Q_f^T X = [x_{i_1} - x_{j_1} + I_1, \; x_{i_2} - x_{j_2} + I_2, \; \ldots, \\ &\qquad x_{i_{fs}} - x_{j_{fs}} + I_{fs}, - x_{i_{fs+1}} + x_{j_{fs+1}} - I_{ss+1}, \\ &\qquad - x_{i_{fs+2}} + x_{j_{fs+2}} - I_{ss+2}, \ldots, - x_{i_f} + x_{j_f} - I_s]^T \end{aligned} \tag{20}$$

where the **faulty set** F represents the set of all the stuck faults and S_F is an $(l+s)xf$ matrix while l_F is an $fx1$ vector.

Now (17) can be re-written as

$$\Delta X = S_F \, l_F \tag{21}$$

The remaining work is to analyze this equation by limited measurements of circuit responses. Assume that the first m elements of ΔX can be measured and $f + 1 < m < s$, we obtain

$$\begin{bmatrix} \Delta X^M \\ \Delta X^{L+S-M} \end{bmatrix} = \begin{bmatrix} S_{MF} \\ S_{L+S-M,F} \end{bmatrix} l_F \tag{22}$$

where M represents the set of measurements. Thus, the following **test equation** is obtained by only considering the first part of the above equation:

$$S_{MF} \; l_F = \Delta X^M \tag{23}$$

Here S_{MF} is an mxf matrix whose columns correspond to the stuck faults in the CUT. Similarly S_{MS} is an mxs matrix whose columns correspond to all of the potential stuck faults in the CUT, where S indicates the set of all potential faults, i.e., all ideal switches. The test equation (23) plays an important role in relating the limited circuit output measurements with the stuck faults in a linear way.

3. STUCK FAULT LOCATION

Fault diagnosis involves three stages: fault detection, fault location and parameters verification. Fault detection is accomplished by measuring circuit responses. If the measurements deviation vector ΔX^M is zero, the CUT is judged fault-free for the given measurement set. Otherwise, at least one fault is detected.

To locate the stuck faults in the CUT, let us analyze the test equation. The right-hand side of (23) is a known vector and the left-hand side is the product of an unknown coefficient matrix S_{MF} and an unknown solution vector l_F. Note that matrix S_{MF} is the set of selected columns of the known matrix S_{MS}. The columns of S_{MF} correspond to the locations of switches, i.e., the stuck faults while the columns of S_{MS} correspond to the locations of all inserted switches. And matrix S_{MS} has more columns than rows since $m<s$ by restriction in Section 2. Our idea to identify the faults is to identify the minimum size ambiguity group in the test equation by finding the minimum number of independent columns in matrix S_{MS} that satisfy the test equation. A recently developed numerically efficient approach [8-10] to multiple analog fault diagnosis is utilized here to identify the stuck faults.

An important observation is that the process derived in part 2 only considers the stuck-at, bridging and stuck-open faults ignoring circuit parametric deviations for simplicity. Hence, parameter verification is omitted and only fault detection and location are discussed here. However, the proposed approach can be applied to the mixed fault condition – multiple stuck-at, bridging, stuck-open faults and multiple parametric faults. Test equation (23) still holds while only the structural matrices A, A_f must be expanded to include the parametric faults. Consequently, the parameter verification is required after the fault location. Future work on this method will include these parametric faults.

4. EXAMPLE CIRCUIT

The classical Fairchild µA741 operational amplifier is selected to demonstrate the proposed method. A simplified schematic of µA741 is shown in Fig. 2.a [11]. The negative feedback configuration is the circuit under test [Fig. 2.b] with a small signal voltage input $V_{in}(t) = 0.01 \sin 120\,pt$. The small signal model of bipolar junction transistors (BJT) in Fig. 2.c is applied to all 18 BJTs for simplicity. There are 21 nodes, 48 resistors, and 18 voltage-controlled-current sources in the CUT. The nominal values of circuit parameters are indicated in figures. Note that the external potentiometer R_{EXT} in Fig. 2.a is equally divided into two resistors with a value of $5kW$.

For simplicity, we only consider 5 suspicious stuck-at-0 faults that are located between node pairs {9, 0}, {12, 0}, {13, 0}, {15, 0}, {17, 0}. Thus 5 open ideal switches are inserted between these nodes pairs. The first two ideal switches are supposed to be closed in the faulty circuit. Nodal voltages are measured at nodes {3, 6, 14, 16}. Hence, $n=20$, $f=2$, $s=5$, $m=4$ and $f+1<m<s$. The measured nodal voltage deviations are

$$\Delta X^M = \begin{bmatrix} -4.4781 & e-004 \\ -2.8747 & e-003 \\ -7.8085 & e-003 \\ -4.3321 & e-002 \end{bmatrix}$$

which obviously is not a zero vector indicating faults detected.

Applying the ambiguity group locating technique to the test equation, a $3x2$ matrix C is obtained after Gaussian elimination and QR factorization with column permutation {3, 2, 4, 1, 5}:

$$C = \begin{bmatrix} 1.6679 & e-015 & 5.1167 & e-004 \\ 4.3052 & e-003 & 1.1034 & e-002 \\ -1.6813 & e-013 & -5.1821 & e-002 \end{bmatrix}$$

Thus the basis of ambiguity group is {3, 2, 4} which correspond to the 3rd, 2nd, and 4th switches respectively. The co-basis is {1, 5} corresponding to the 1st and 5th switches.

By analyzing matrix C, there is only one suspicious ambiguity group {1, 2}. According to the procedure in Section 4 in [10], this is the minimum size ambiguity group. We conclude that switches {1, 2} are closed, i.e., there are two stuck-at-0 faults on nodes pairs {9, 0} and {12, 0}, which are the exact solutions for this CUT.

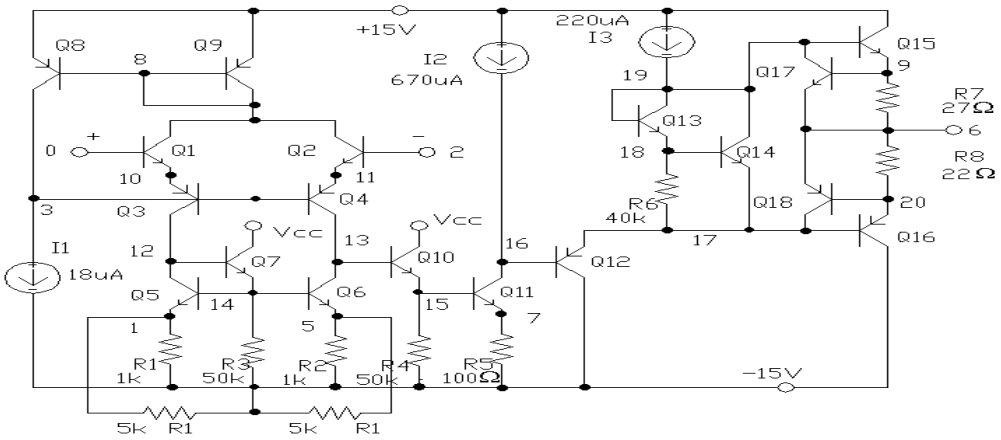

Figure 2.a overall schematic of the Fairchild µA741 operational amplifier.

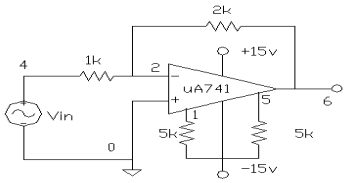

Figure 2.b Negative feedback configuration of µA741.

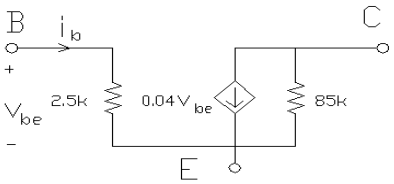

Figure 2.c The small signal model of BJT.

5. CONCLUSIONS

Although analog and mixed signal test and fault diagnosis are less advanced than digital test, digital test techniques greatly influence the analog test. As a widely used paradigm in digital test, stuck-at model together with the output monitoring has been applied to analog area to model the open or short failure mechanisms. These fault models are increasingly important for today's systems-on-chip solutions with increased complexity and increased die size of analog and mixed signal designs. In this paper, such models are utilized to locate faults by verification approach rather than by dictionary approach typically used in such case. With the known circuit topology, the ideal switches are inserted to connect the suspicious circuit nodes. Under normal conditions, all ideal switches are open (closed) while some of them are closed (open) under faulty conditions. The circuit topology is modified by the inserted switches and new modified nodal equation is established based on KCL equations. Test equation relates the limited measured circuit responses with the faults in a linear way. A recently developed numerically efficient approach to multiple fault diagnosis is applied to identify the faults. Ambiguity group locating technique based on the QR factorization is utilized to identify the minimum number of faults satisfying the test equation. The number of measurements is less than the number of inserted ideal switches, but it is greater than the number of faults plus one. Avoiding the combinatorial search of suspicious stuck-at and stuck-open faults reduces computation cost of multiple fault location. The proposed method can also be applied to the mixed faults condition – multiple stuck-at, bridging and stuck-open faults together with the multiple parametric faults. Finally, a commercial analog IC is provided as an example to demonstrate the proposed method.

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