A DYNAMICALLY RECONFIGURABLE SYSTEM-ON-A-CHIP ARCHITECTURE FOR FUTURE MOBILE DIGITAL SIGNAL PROCESSING

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ABSTRACT

The evolving of current and future broadband access techniques into the wireless domain introduces new and flexible network architectures with difficult and interesting challenges. The system designers are faced with a challenging set of problems that stem from access mechanisms, energy conservation, error rate, transmission speed characteristics of the wireless links and mobility aspects. This paper presents first the major challenges in realizing flexible microelectronic system solutions for digital baseband signal processing in future mobile communication applications. Based thereupon, the architecture design of flexible *system-on-a-chip* solutions is discussed. The focus of the paper is the introduction of a new parallel and dynamically reconfigurable hardware architecture tailored to this application area. Its performance issues and potential are discussed by the implementation of a flexible and computation-intensive component of future mobile terminals.

1 INTRODUCTION

Flexible future mobile communication systems open a set of challenging problems to system designers in the wireless industry. The requirement of future generations mobile terminals can be summed in dynamic flexibility, higher performance and less power consumption compared to current terminals. The combination of advances in integrated circuit technology and novel system-level solutions can contribute efficiently to the widespread commercialization of mobile high-speed communication systems. Future mobile communication systems, e.g. third generation (3G) systems, will offer many new exciting services, which will range from internet browsing to real-time multimedia communication applications. Thus, the design of a corresponding mobile system has to reflect all these forecasted services, data rates and flexibility. At the same time the mobile devices should realize all services within the physical and operational requirements of the given mobile system infrastructure. Finally, the *time-to-market* and low price requirements have to be fulfilled in order to be competitive. This results in the following two major requirements:

- a new efficient system model in 3G systems, e.g. CDMA-based transmission schemes being highly flexible and adaptable to new services [3], and
- new innovative flexible microelectronic design solutions.

Currently, most of the microelectronic system solutions in mobile communication are a combination of ASICs, microcontrollers, and Digital Signal Processors (DSP) devices. Universal reconfigurable hardware architectures have been proven in different application areas [1] [2] [5] to produce at least one order of magnitude in power reduction and increase in performance, e. g. for implementing filters, correlators, multipliers etc. The new coarse-grained reconfigurable architecture introduced here promises for the selected application area more flexibility than ASICs and better performance values than DSPs or even today´s fine-grained commercial reconfigurable devices [10]. Thus, one important goal is to evaluate flexibility versus power/performance trade-offs by releasing the DSP for other tasks, or by migrating functionality from ASICs to the coarse-grained reconfigurable hardware supporting the implementation of highly efficient *System-on-a-Chip* (SoC) solutions for hand-held devices in mobile communication systems [7]. For computation-intensive arithmetic-dominated functions with flexibility [11] [12] requirements found in mobile communication applications, reconfigurable hardware offers a needed extension to the software programmable DSPs, e. g. for realizing promising concepts such as *Software Radios* [4] [6]. Target SoC architectures may be composed of different cores such as DSPs, microcontrollers and memories, as well as of reconfigurable hardware and/or various ASIC support parts. An overview of a possible hardware/software SoC architecture related to a *Baseband Single Chip Mobile Transceiver* is shown in figure 1, addressing layer 0 (L0) and layer 1 (L1) hardware operations, e.g. channelization, detection, decoding etc. In the application area viewed here, new upgrades, services or protocols could probably be downloaded from the internet for configuring the hand-held devices according to these downloaded codes. In addition, future mobile terminal should be able to support many modes of operation, e g. voice, audio, video, navigation, data transmission etc. This means for example

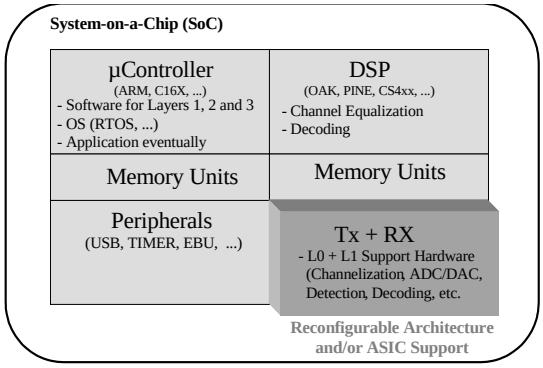


Figure 1 SoC-Architecture Components of a *Baseband Single Chip Mobile Transceiver*

also, that the mobile device has to have the ability to operate within different standards, such as GSM, UMTS and IS-95. Thus, such mobile terminals could adapt easily and quickly to new services and standards by reconfiguration.

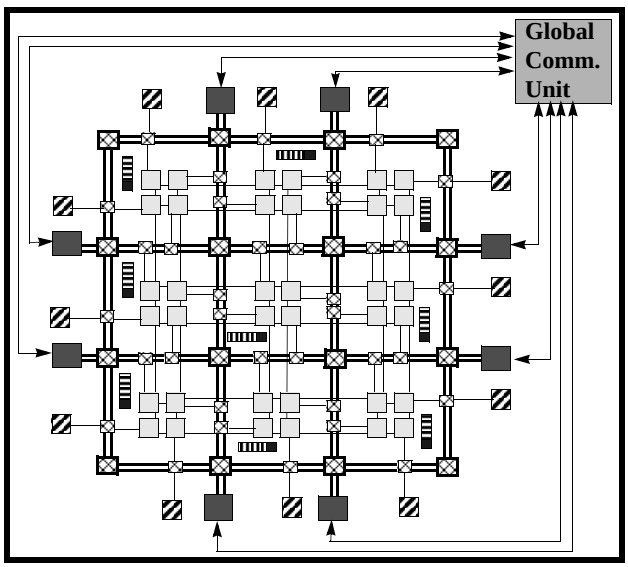
The paper is structured as follows: in section 2 a detailed description and introduction of the proposed dynamically reconfigurable parallel hardware part of such SoCs is provided, including its evaluated performance issues and implementation status. The usefulness of this new coarse-grained array architecure is illustrated in section 4 by the implementation analysis of a computation-intensive application part in future mobile terminals, e. g. a flexible CDMA-based RAKE-receiver.

2 A COARSE-GRAINED DYNAMICALLY RECONFIGURABLE HARDWARE ARRAY

For preparing future mobile terminals and its microelectronic components to cope with all the challenges described above, we developed a new coarse-grained and dynamically reconfigurable architecture. The integration of this application-tailored but flexible hardware architecture within flexible SoCs solutions for digital baseband processing will support the efficient realization of the mentioned features. The proposed *Dynamically Reconfigurable Architecture for Mobile Systems (DReAM)* consists of an array of concurrently operating coarse-grained *Reconfigurable Processing Units (RPUs)*. Each RPU is designed for executing all required arithmetic data manipulations for the data-flow oriented mobile application parts, as well as to support necessary control-flow oriented operations. The complete DReAM array architecture connects all RPUs with reconfigurable local and global communication structures (see figure 2). In addition, the architecture will provide efficient and fast dynamic reconfiguration possibilities for the RPUs as well as for the interconnection structures, e.g. only partly and during run-time while other parts of the reconfigurable architecture are active. In the following, the design, structure and performance issues of the major hardware components in the DReAM architecture are explained briefly. For more information on DReAM and details about all operation´s performance values see [7].

The decisions during the design of the architecture were mainly based on the careful reviewing of the tailored application area requirements, e. g. on the study of different algorithms needed in future mobile transceivers incl. their operations and implementation precision. Examples for such complex algorithms, requiring also flexibility in execution, are RAKE-receiving parts, interpolation filtering, searcher and synchronization algorithms, coding and modulation techniques etc. Based on the set of used arithmetic and control-flow operations the performance/power optimized structure development of the RPUs, and of so-called *Communication Switching Units (CSUs)* was done. As shown in figure 2, the DReAM architecture consists of a scalable array of RPUs that have 16-bit fast direct local connections between neighbouring RPUs, whereas each sub-array of four RPUs shares one common *Configuration Memory Unit* (CMU). The CMU holds configuration data for performing fast dynamic reconfiguration for each of these four RPUs and is controlled by one responsible CSU. Each CSU controls two CMUs and four global interconnect *Switching Boxes* (SWB). All CSUs communicate to one *Global Communication Unit* (GCU), which coordinate centralized all dynamic reconfiguration steps, e. g. of the RPUs as well as of the global interconnection structure. Moreover, the GCU controls the external communication with other hardware components of the flexible SoC. Therefore, *Dedicated I/O Units* (DIOs) for fast and parallel transfers of input/output data are placed around the array architecture.

The dynamically *Reconfigurable Processing Units* (RPUs) are the major hardware components of the DReAM



Legend:

- Reconf. Proc. Unit (RPU).
- Dedicated IO (DIO).
- Comm. Switching Unit (CSU).
- Configuration Memory Unit (CMU) and its Controller.
- Switching Box (SWB).
- RPU to Bus Connection point.
- 16-Bit Global Interconnect Line.
- 16-Bit Local Interconnect line.

Figure 2: Hardware Structure of the Dynamically Reconfigurable DReAM Architecture

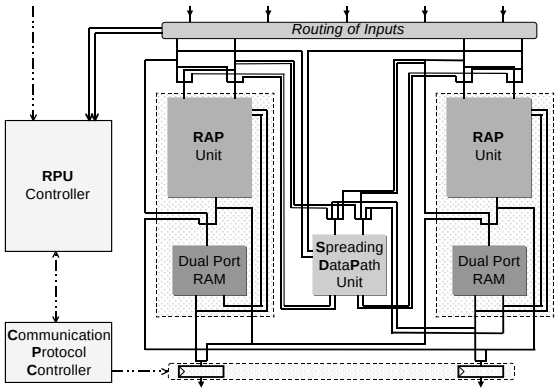


Figure 3 Hardware Structure of the *Reconfigurable Processing Unit* (RPU)

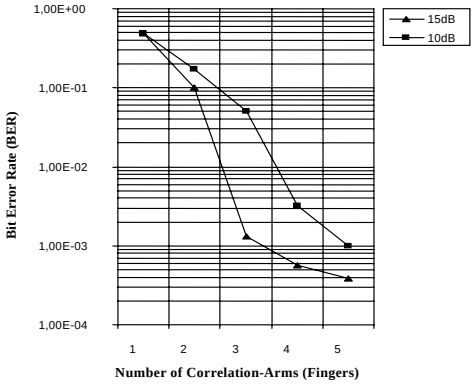


Figure 4: Bit-error-rate (BER) as function of number of fingers in the RAKE-Receiver

architecture for executing the arithmetic-dominated data manipulations. Thus, these application-tailored RPUs perform efficiently the required coarse-grained (8-/16-bit) integer operations needed for the examined application parts. In contrast, the CLBs (*Configurable Logic Blocks*) of today´s commercially available fine-grained and universal FPGA-chips are operating on the 1-bit level [10]. In figure 3 is shown, that each RPU consists of:

- two dynamically reconfigurable 8-bit data paths, (*Reconfigurable Arithmetic Processing Units*, RAPs),
- one *Spreading Data Path* (SDP),
- one *RPU-controller*,
- two *dual port RAMs*, and
- one *Communication Protocol Controller*

Each RAP can perform all necessary arithmetic operations (8-/16-bit) identified in the above mentioned examined application parts of mobile communication systems. The available set of two-input operations supports either operations with one constant operand (fixed Y), as well as operations with two variables as inputs (variable Y). The RAP unit is built around a fast integer multiplier operator, providing a high speed constant/variable multiplication and small compact design by using modified Look-Up Table (LUT) multiplication procedure applying distributed arithmetic. According to [11] most of the multiplication within the mobile system are fixed operand operation. One *Spreading Data Path* (SDP) for fast and efficient execution of CDMA-based spreading tasks is designed and implemented in each RPU. This SDP unit can be used together with the 2 RAPs for implementing efficiently fast complex PN-code correlation operations. The *RPU-controller* is responsible for guiding all data manipulations and transfers inside the RPU. Moreover, the *RPU-controller* performs, together with the CMU, the fast dynamic reconfiguration of RPUs. For details about efficient communication and dynamic reconfiguration mechanisms see [13].

3 APPLICATION MAPPING: FLEXIBLE CDMA-BASED RAKE-RECEIVER

The following example of a computation-intensive RAKE-receiver component from future mobile communication systems will be mapped manually onto DReAM. The goal of our approach is to map selected application parts onto the reconfigurable SoC-part, which are too complex for the DSPs, especially for low power DSPs with reduced clock rates, but which still require operation flexibility, so that ASIC implementations would be not sufficient. For future CDMA-based mobile communication systems RAKE-receivers are essential while consuming a huge computation performance [11]. ASIC implementations could provide such a performance, but are not flexible enough to adapt to the various situations and services in the next generation of wireless communication systems. Another important point is the *risk minimization* by the implementation flexibility of reconfigurable hardware, which is very important, especially in the case of late specification changes, or different and changing standards.

In DS-CDMA systems the data signal is multiplied by a PN sequence with much higher bandwidth than the one of the data signal. Thus, the Spread Spectrum (SS) signal is well matched for multipath channel. i.e. more than one copy of the transmitted signal will arrive at the receiver with different time delays. If the time delay between the received copies is more than one chip duration, then a RAKE-receiver (with n fingers, where n is the number of different path signals) can resolve and then combine the signals according to their SNR. The received data signal for each finger can be found as a complex correlation (QPSK-modulation) of the binary delayed signal y(t) and the conjugate of the PN-code (*pn**):

$$r = \sum_{n=0}^{L-1} \int_{0}^{T} y\left(t - \frac{n}{W}\right) c_n^*(t) pn^*(t) dt$$

where *cn** is the complex conjugate of the weighting factor for each finger.

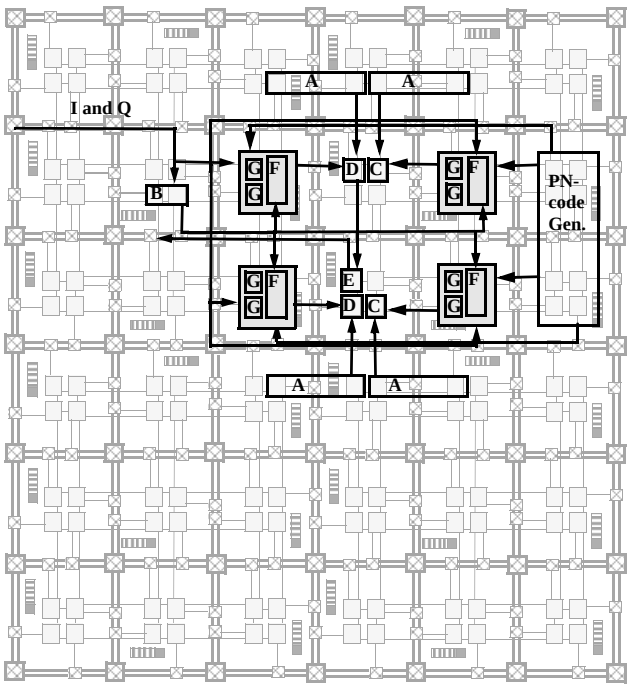
A RAKE-Finger despread the received signal with a correlator. The despreaded signal is then multiplied by a complex amplitude to correct phase-error and to weight each finger according to *Maximal-Ratio-Combining* (MRC) strategy. The number of Rake-fingers depend on the channel-profile and the chip-rate, e. g. the higher the chip rate, the more resolvable paths. IS-95 uses RAKE-receivers with four fingers [12]. We used MATLAB 5.2 for simulating a RAKE-Receiver with variable number of fingers for the

high data rate required in the third generation standard (1.5 Mbs). Assuming, there is ADC that can support that high sampling rates, figure 4 shows the effect of increasing the number of fingers on the performance of the receiver, the lower bit-error rates (BER).

Hardware Function.	Required performance [Mhz]	DReAM Performance available
Dual Port RAM	96	120
Spreader	24	120
Adder	24	120
Accumulator	72	100

Table 1: RAKE-Receiver Performance Issues

In addition, the simulation results show that 8-bit quantization produces more than three times improvement over 4-bit quantization. RAKE-Receiver implementation with 4 fingers, which was performed onto the DReAM hardware array architecture. For the required data symbol rate of 32 Msymbols/s, i.e. one symbol (8-bit) is arriving every 0.125 microseconds, it can be seen that DReAM can provide an acceptable performance for such high data rates (see Table 1). One possible mapping of the front-end of the CDMA-based RAKE-Receiver onto the dynamically reconfigurable DReAM hardware array is provided in figure 5.



A: Channel tracker, which provide the gains of each finger (Ci)
B: Channel sounding allocating 2 correlators to scan the impuls response
C: Multiplier.
D: Multiplier and adder.
E: Adder.
F: RAM
G: Correlator.

1 RAKE-finger

Figure 5: Rake-Receiver example mapped to the DReAM Array Architecture.

Conclusion

The paper presented first an overview of the challenges in realizing flexible microelectronic system solutions for future mobile communication applications, e. g. *system-on-a-chip* (SoC) solutions for digital baseband processing in mobile radio devices. This paper introduced a new coarse-grained dynamically reconfigurable architecture (DReAM), including its potential for SoC-solutions in adaptive air interface candidate systems for future generations of wireless communication systems. DReAM is tailored to future mobile signal processing, providing an acceptable trade-off between flexibility and application performance requirements. The goal is to map those application parts onto the reconfigurable architecture, which are too complex for the DSPs, especially for low power DSPs with reduced clock rates, but which still require different types of flexibility, so that ASIC implementations would be also not sufficient. Future CDMA-based mobile communication systems have a huge potential for such application parts as shown by the DReAM implementation of a CDMA-based RAKE-receiver. Aspects like *risk minimization* and *time-to-market* are very important, especially in the case of late specification changes (standards!).

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