Cost-Oriented Design of a 14-bit Current Steering DAC Macrocell

Janusz A. Starzyk
Ohio University
starzyk@bobcat.ent.ohiou.edu

Russell P. Mohn
Sarnoff Corporation
rmohn@sarnoff.com

Abstract

This paper presents the design concept and implementation of a 14-bit current steering DAC macrocell for a SOC in 0.13um CMOS. The design approach minimizes total fabrication cost of the SOC. The paper demonstrates that using this approach smaller and economically efficient DACs will result without a loss to specified design requirements.

1. Introduction

Designs for modern communication hardware, e.g. broadband modems for new communication standards and wireless communication systems, require high performance at a low cost. Integration of digital and analog components on a single chip is a recommended system level solution and this makes design of mixed-signal macrocells, e.g. a digital-to-analog converter (DAC) even more challenging than design of stand alone components. Chip size is of critical importance due to high cost and low yield of the manufacturing process for advanced system on a chip (SOC) solutions.

This paper presents a cost-oriented design of a current steering 14-bit DAC macrocell to be integrated in a SOC with other mixed signal and digital parts. Core macrocells like this one can be reused in different SOCs lowering the design cost and increasing the system integration level. At the same time, the designed part must satisfy high speed and high accuracy requirements in addition to linearity and spurious free dynamic range requirements. The current steering DAC architecture was chosen because of its ability to directly drive a load resistance.

Several recent papers [1-5] addressed current steering CMOS DAC design and discussed various problems as well as suggested recommended solutions. Typically current steering DACs are designed using a segmented architecture in which input bits are divided into two groups with lower significance bits switching the binary coded current sources and higher significance bits switching thermometer coded unary current sources [5]. Both binary and unary sources use matched transistors where the transistor area is designed using statistical process parameters, e.g. S_β and A_β, to attain a desired accuracy. In addition, the current sources are split into 4 or 16 symmetrical locations. They are switched with a 2-dimensional common centroid scheme to minimize the effect of the systematic errors like temperature and electrical gradients and process variations.

One of the critical design parameters for the current steering DAC is its integral nonlinearly (INL) defined as the maximum deviation between DAC output values and the reference straight line from the smallest to the largest output value. INL is related to other important DAC specifications like the spurious free dynamic range (SFDR) and the output impedance. In statistical design of a current steering DAC, the INL is related to the area of current source transistors, and for increase in DAC precision by one bit the area must increase 4 times. The INL yield can be calculated as described in [3]. Assuming that the INL and fabrication yields are independent, we can consider total design yield as a product of the manufacturing and INL yields. Since increasing the current source transistor area increases the INL yield and at the same time decreases the fabrication yield, an optimum design can be found for which the largest number of manufactured DACs satisfy the design requirements. Our design was based on this approach.

In Section 2 the statistical yield model is reviewed emphasizing the effect of the design area on the systematic errors. Section 3 presents techniques used to reduce the effect of systematic errors while Section 4 discusses combined effect of the manufacturing and the INL yields and relates them to the total fabrication cost. It shows that there is an optimum size for DAC design area that is necessary to satisfy design objectives at the lowest cost. Section 5 discusses DAC implementation in 0.13μm CMOS technology and presents the designed DAC performance figures. Finally, the conclusion is given in Section 6.

2. Statistical Yield Model

Random mismatches of the current source transistors contribute to the INL of DACs. A statistical model that formulates the INL level given the current source accuracy was derived in [3]. Based on this model one can obtain required current source accuracy and subsequently the required design area of the current source transistors as described in [6].

$$A = \frac{1}{2\left(\frac{\sigma(I)}{I}\right)^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)_{CS}^2}\right] \quad (1)$$

where $\frac{\sigma(I)}{I}$ is the relative standard deviation of the matched current sources, and A is the current source transistor area.

In general, larger A means the current sources are more precise and better matched. However, at some point the systematic errors caused by process, temperature, and electrical gradients will reduce the effectiveness of this technique. The systematic errors are minimized with layout techniques like splitting the current source transistors and placing them in symmetrical locations with a common centroid and switching them in an optimal order. For instance, a random walk switching scheme is presented in [5].

The level of systematic errors can be determined by linking the total area of the current source array to relative standard deviation of the matched current sources expressed by

$$\left(\frac{\sigma(I)}{I}\right)^2 \approx \frac{1}{2A}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)_{CS}^2}\right] + S_\beta^2 D^2 \quad (2)$$

The worst case mismatch occurs when transistors are spaced by $D = \sqrt{\frac{A_{tot}}{2}} = k\sqrt{2^{N-1}A}$, where $k=A_{cell}/A>1$ is a current cell layout coefficient, . A_{cell} is the unit current cell area, and N is the number of bits the converter can resolve. Therefore, the worst case standard deviation with systematic errors of the matched current sources is determined by

$$\left(\frac{\sigma(I)}{I}\right)_{comb} \approx \sqrt{\frac{1}{2A}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)_{CS}^2}\right] + S_\beta^2 k^2 2^{N-1} A} \quad (3)$$

For a smaller resolution DAC, the systematic errors are not so important. However for a 14-bit DAC, the effectiveness of reducing mismatch errors just by increasing the current source transistor area is questionable because the term $S_\beta^2 k^2 2^{N-1} A$ grows quickly and dominates the current source deviation. Increased spacing, which results from larger transistor area and the number of transistors used, increases the mismatch between current source transistors. In addition, increase in area means the SOC will be more costly to fabricate. Therefore, the reduction of the systematic errors by appropriate switching technique is recommended.

3. Reduction of Systematic Errors

By splitting the unary current source transistors symmetrically into several locations we can eliminate the systematic linear errors and reduce the quadratic errors. To compensate for linear errors a symmetrical splitting is required with respect to both axes (see Fig. 1); therefore, each transistor will be split into 4 locations. As a result all linear errors are completely compensated. Optimizing the switching scheme and switching sequence reduces quadratic systematic errors.

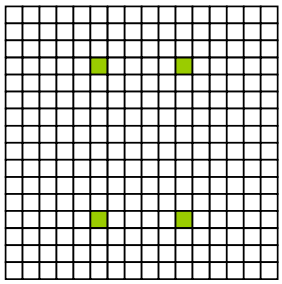

Fig. 1 Compensation of the linear errors by splitting the unary current sources

Quadratic error compensation by symmetrical selection sequence was inadequate as was indicated in [4] with the INL error growing as

$$INL = 2^{N/2} k S_\beta D[LSB] \quad (4)$$

In [5] a Q^2 random walk encoding was developed where the thermometer encoded bits are divided into two groups

1) the most significant group and
2) remaining bits (other than those used in the binary section.)

The switching scheme in [5] is referred to as quad quadrant or Q^2 as four units in every quadrant compose one current source to make an 8-bit thermometer array as illustrated in Fig. 2. Q^2 Random Walk was used in [5] together with splitting of the unary sources into 16 cells.

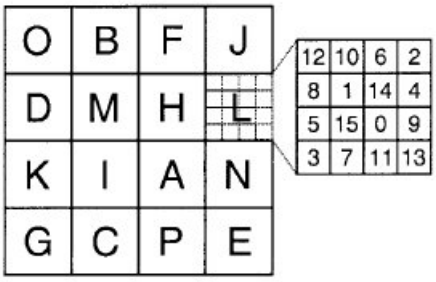

Fig. 2 Q^2 random walk switching sequence in 8-bit thermometer DAC

In this work a new **optimized permuting algorithm** capable of reducing the systematic errors to a minimum was developed. Switching begins with the transistor block at the point in 2-D space where the estimated quadratic error of unit current sources have a value equal to half of the spatial average of all the current sources in the array. Selection continues at 2-D symmetrical positions, selecting unary current sources in a specific sequence. This approach requires two-level thermometer

encoding that yields a simplified implementation of the encoding logic. For encoding 8-bits into thermometer code, 3-bit and 5-bit thermometer encoder sections are needed.

4. Design Cost Consideration

Using results from [3] the relationship between $\frac{c(I)}{I}$ and the INL for a 14 bit DAC is as shown by the upper (dashed) curve in Fig. 3

For instance, to achieve 99.8% INL yield the standard deviation of the current sources must be set to 0.12%. This approach was taken in most of the designs reported in the literature. There was no justification why the 99.8% INL yield level was targeted. Is it true that higher INL yield means a better DAC? Certainly not. No one suggests a design with 100% INL yield for his design and for a good reason. It would be too expensive.

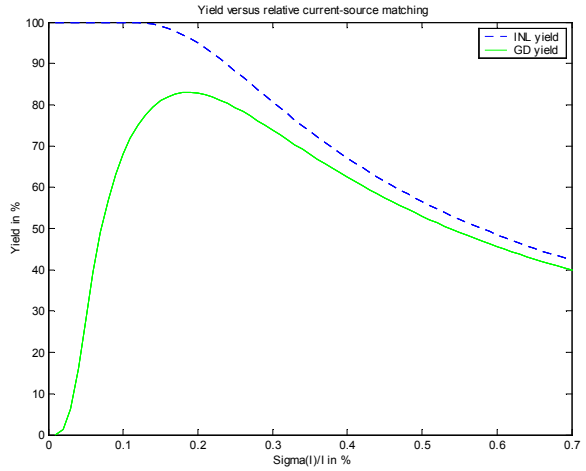

Fig. 3 Yield as a function of the current source matching

While using $\frac{c(I)}{I} = 0.12\%$ will guarantee that 99.8% of fabricated and functional DACs would meet the INL design specification it does not mean that an overall optimum was reached with respect to the combined effect of fabrication defects and the INL yield. One obvious reason for this is an increase in the design area associated with meeting the INL requirement. Increased DAC area would result in larger size of the fabricated chips and lower manufacturing die yield. For a given technology with a fixed number of statistical defects per unit area D the manufacturing die yield can be estimated from:

$$\text{Die yield} = \left(\frac{1 - \exp(-AD)}{AD} \right)^2 \qquad (5)$$

Where A is the die area. By taking a product of the INL yield and the manufacturing die yield we can define the good die yield (GDY). GDY reveals the percentage of the manufactured dies that will work according to specifications. (see the lower curve on Fig. 3) As we can see from Fig. 3 the optimum $\frac{c(I)}{I}$ which maximizes GDY is ≈ 0.2%, a significantly **larger** value than that which guarantees 99.8% INL yield.

If the yield figure is related the overall design area we may observe that the maximum yield corresponds to the DAC area of 5 mm^2 as is illustrated on Fig. 4.

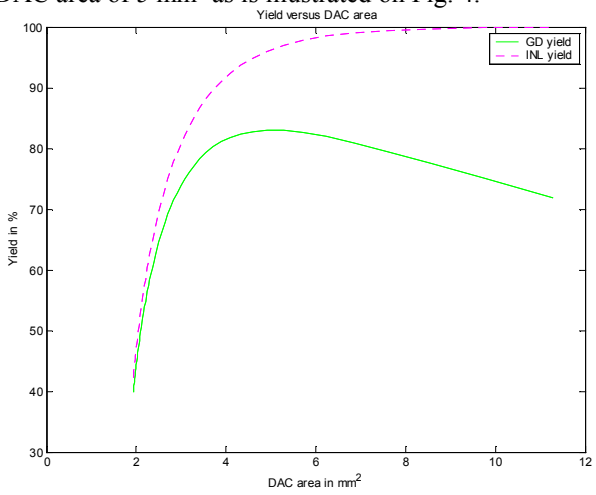

Fig. 4 Yield as a function of the DAC design area

Finally, if we consider the cost criteria of the SOC fabrication (chip cost increases at least proportionally with the chip area) than the effective cost per working SOC is as illustrated on Fig. 5 with the optimum DAC area less than 4 mm^2.

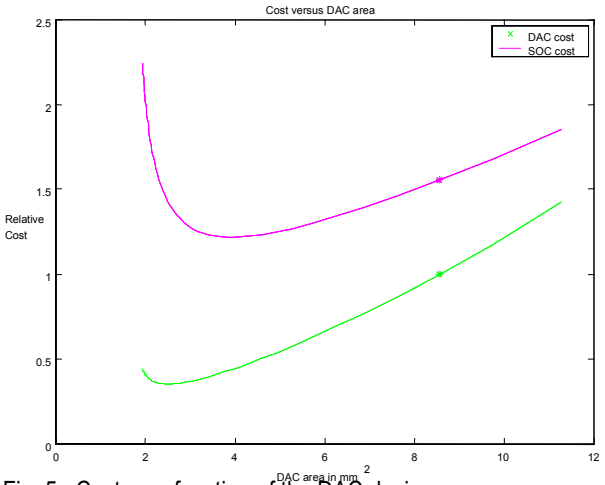

Fig. 5 Cost as a function of the DAC design area

Cost numbers shown in Fig. 5 are relative to the cost of fabricating a single DAC macrocell designed to satisfy 99.8% INL requirements (marked with * - the DAC design area 8.55μm^2). We can see that using cost oriented design we can reduce the fabrication cost more than 2 times (the lower curve on Fig. 5).

Similar results are obtained if the DAC is fabricated as a macrocell on SOC. Since SOC digital subsystems to

be integrated with our design were using 16 mm^2, the combined effect of the DAC design area and the remaining SOC parts area have to be considered in implementing the optimum size strategy. The combined fabrication cost for the SOC with the DAC as a function of the DAC area is illustrated by the upper curve on Fig. 5. As we can see from this figure, the overall SOC cost can be reduced by 21% if the DAC is designed with the optimum cost approach. Therefore, in a general cost oriented design strategy, DAC size is determined by the combined INL and manufacturing yield statistics, which result in a smaller design area and cost than if the design is solely based on the INL statistics.

5. DAC Implementation

The DAC is implemented as a macrocell in UMC13 0.13μm 6 metal double-poly CMOS to be integrated with other analog and digital parts in a SOC. It uses 3.3V power supply for analog circuits and 1.2V power supply for digital circuits. Analog circuits include the current sources and voltage reference. Digital circuits include flip-flops, thermometer encode circuits, latches, and switches. It is specified to operate from –40°C to 125°C. The macrocell is integrated with the voltage reference bandgap circuit that provides stable voltage independent of changes in the power supply and temperature. A self-reference circuit adjusts the reference current to the analog power supply in order to maintain constant output current. It uses 8-bit thermometer, 6 bit binary coding, composite current source transistors splitting into 4 sections and a customized switching scheme. The macrocell dimensions are 1700 μm x 1716μm for the total design area of 2.918 mm^2. The layout of the macrocell is shown on Fig. 6. It delivers the maximum full-scale current of 20 mA, to two differential load resistors of 75 Ω each. Maximum differential output voltage is 1.5 V on each load resistor. Power dissipation at the full-scale current is below 90 mW at all operating conditions.

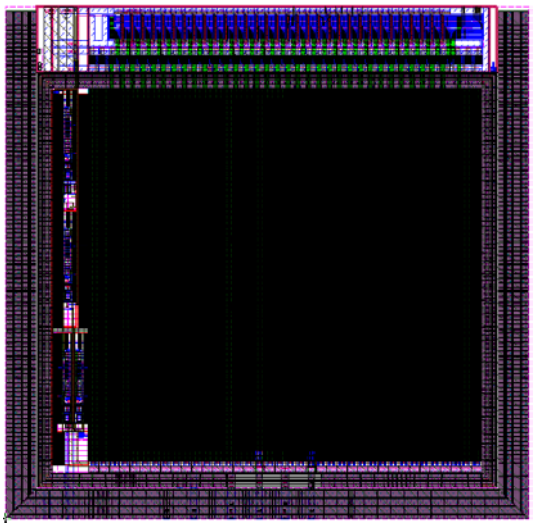

Fig. 6 14-bit DAC macrocell layout

6. Conclusion

In this paper we demonstrated that using a cost-oriented approach to DAC macrocell design results in a smaller size layout. In this approach, systematic errors are less severe than in the traditional design approach based on maximizing the INL yield. The smaller size and minimization of systematic errors result in a higher yield for SOCs that integrate this DAC macrocell.

References

[1] R. Jacob Baker, Harry W. Li and David E. Boyce, "*Cmos Circuit Design, Layout, and Simulation*" New York, IEEE, 1997, p. 802-804

[2] A. Van den Bosch, et al. "A 10-bit 1-Gsamples/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 315-324, Mar. 2001.

[3] A. Van den Bosch, et al. "An Accurate Statistical yield model for CMOS current-steering D/A converters," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2000, pp. IV.105-IV.108.

[4] J. Bastos et al., "A 12-bit intrinsic accuracy high-speed CMOS DAC "IEEE Journal of Solid-State Circuits, Vol.: 33 Issue: 12, Dec. 1998 pp. 1959 –1969

[5] G.A.M.Van Der Plas, et al. "A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC," *IEEE Journal of Solid-State Circuits,* Vol. 34 Issue: 12, Dec. 1999 pp. 1708 –1718

[6] M. Pelgrom et al., "Matching Properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-24, pp. 1433-1439, Oct. 1989.

[7] J. Vandenbussche et al., "Systematic design of a 14-bit 150-MS/s CMOS current-steering D/A converter," *Proc. Design Automation Conference, 2000*, pp. 452- 457.

[8] A. Van den Bosch, et al. "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," Proceedings of The 6th IEEE International Conference on Electronics, Circuits and Systems, ICECS '99, Vol. 3, 1999, pp. 1193 –1196.