ANALOG VLSI DESIGN OF MULTI-PHASE VOLTAGE DOUBLERS WITH FREQUENCY REGULATION

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ABSTRACT

This paper proposes a new organization of charge pump circuits based on a voltage doubler [2] that takes a DC input and outputs a doubled DC voltage. By cascading n multi-phase voltage doublers (MPVD), the resulting charge pump has the voltage gain equal to 2^n. It needs n clock pairs to control the pumping process. MPVD is a minimum capacitance realization of the switched-capacitor based voltage doubler. An n-stage MPVD needs n+1 capacitors and 2n switches. To avoid the short circuit during switching, a clock pairs generator is used to achieve multi-phase non-overlapping clock pairs. A frequency regulator is designed to lower the charging frequency when the load becomes lighter, thus reducing the power loss during switching. A 2-stage MPVD is implemented in the Orbit 2.0μm analog CMOS technology. The simulation results show that the output voltage is 3.995 times the power supply. By using the frequency regulator, the power efficiency is dramatically improved when the load becomes lighter.

I. INTRODUCTION

A DC-DC charge pump circuit provides a DC voltage that is higher than the DC voltage of the power supply or provides a voltage of a reverse polarity. In many applications such as Power IC, continuous time filters, and EEPROM, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers. For that reason, a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited.

Existing charge pumps such as Dickson [1] and Makowski [3] charge pumps require a two-phase clock to control the charge transferring between capacitors. The voltage gain of a charge pump is a function of the number of stages in the pump. An n-stage Dickson pump has a voltage gain equal to n+1. In [3], Makowski established a theoretical limit on the voltage gain in a two-phase multiplier and related it to Fibonacci numbers. An n-stage Makowski charge pump has a voltage gain equal to the 2nth Fibonacci number. Makowski's charge pumps have the highest voltage gains, which need the least number of capacitors among two-phase charge pumps. This paper presents a VLSI design of MPVD, which require multi-phase clock pairs and whose voltage gain is higher than the limit set by Makowski.

A 2-stage MPVD is implemented in the Orbit 2.0-micron CMOS technology using MOSIS Fabrication Service [5]. The die size is $2220 \times 2250\ \mu m^2$. To improve the power efficiency, especially in the light load condition, a frequency regulator (discussed in detail in section IV) is used to regulate switching frequency. The power efficiency, driving ability and the frequency regulation are discussed. The schematic design, layout and simulation results presented were obtained using Mentor Graphics tools [4].

II. MULTI-PHASE VOLTAGE DOUBLERS

A switched-capacitor organization of a two-phase DC-DC voltage doubler is shown in Fig. 1. It contains 2 clock-controlled switches and 2 capacitors. VIN is the power supply, and V+ is the voltage output. For a simple explanation of the voltage doubler operation, let us assume that the switches and the capacitors are all ideal. That is, we assume that there is no leakage current in the capacitors, and that the electric charge transferring is instantaneous. Let us assume that the voltage doubler starts in phase I (the two switches are connected to nodes I as shown in Fig. 1). The capacitor C1 is initially charged by the power source to a voltage VIN, and C2 is assumed to have no initial charge. In phase II, the lower voltage terminal C1- of C1 is connected to the power supply. If there were no C2 connected to the higher voltage terminal C1+, C1+ would have a voltage of value 2*VIN. As the C1+ is connected to C2, the charge stored in C1 is shared with C2. The final output voltage V+ is fixed by the VIN plus a voltage due

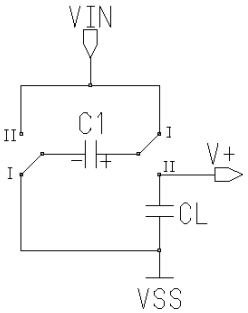

Fig. 1. Voltage doubler

to the final charge in the capacitor C1. This charge is less than the initial one in phase I. The charge redistribution allows V+ to grow. Subsequently, the voltage doubler goes back to phase I, C1 is recharged to hold a voltage VIN, and C2 keeps the previous charge. Then the circuit is switched to phase II again. We obtain a final output voltage V+ value greater than the previous one due to the charge stored in C2. By repeating these operations many times, the output voltage V+ keeps growing to the final voltage 2*VIN.

To achieve a voltage gain higher than 2, we can cascade the voltage doublers as shown in Fig. 2. The resistor RL represents the circuit load. The output voltage of previous voltage doubler is the power supply of the

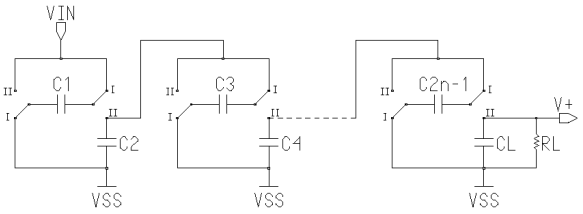

Fig. 2. Two-phase voltage doublers (simply cascaded)

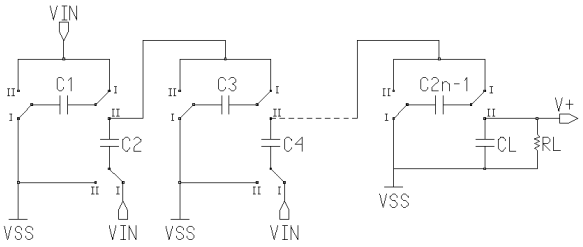

Fig. 3. Two-phase voltage doublers (Makowski charge pump)

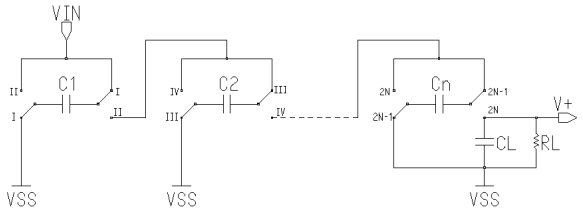

Fig. 4. Multi-phase voltage doublers (MPVD)

next voltage doubler. If there were no load (RL is infinite), the final output voltage is 2^n times the voltage supply in ideal condition (no leakage current), where n is the number of stages of the charge pump. It needs 2n capacitors and 2n switches. Makowski proposed a two-phase charge pump in [3]; the basic diagram of this circuit is shown in Fig.3. An n-stage Makowski charge pump has a voltage gain equal to the 2nth Fibonacci number that is higher than the voltage gain of simply cascaded voltage doublers, and needs 2n capacitors and 3n-1 switches. Starzyk [6] proposed a new multi-phase charge pump shown in Fig. 4. An n-stage Starzyk charge pump has a voltage gain 2^n and it uses n+1 capacitors and 2n switches. It requires n clock pairs to control these switches. Among these three charge pumps, MPVD have the highest voltage gain if the same number of capacitors is used. Hence a desired gain can be implemented with the least design area.

III. 2-STAGE MPVD DESIGN

The basic diagram of the 2-stage MPVD is shown in Fig. 5. The designed charge pump consists of two main parts; one is the 2-stage charging circuit, which delivers charge to the load. The other one is the clock pair generator, which generates the clock pairs used to control the switch of the charge pump. CLOCK is assumed to be available for this MPVD. Input START is used to control starting/stopping of the charging process.

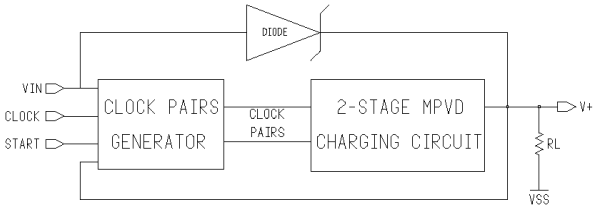

Fig. 5. Diagram of 2-stage MPVD

A. 2-stage MPVD Charging Circuit

The schematic diagram of the designed 2-stage charging circuit is shown in Fig.6. Eight large MOS transistors are designed to control the connection and disconnection of the three capacitors C1, C2 and CL. The clock pairs CK1 and CK2 work at 20kHz, while CK3 and CK4 work at 10kHz. They are used to switch these transistors on and off. The substrates of all the PMOS transistors are connected to the V+, which is the highest voltage in the circuit. To turn these MOS transistors on and off properly, these clock pairs should have an amplitude of V+.

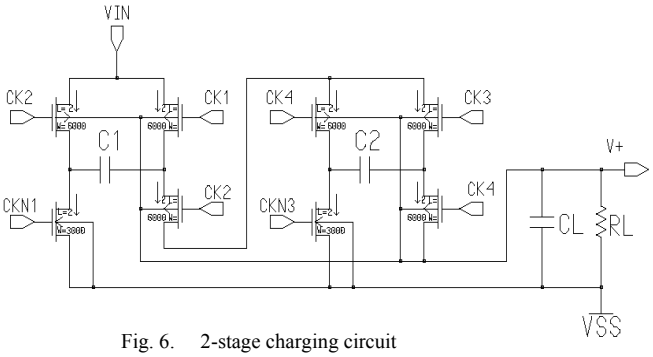

Fig. 6. 2-stage charging circuit

Let us assume that for these large transistors, the turned-off resistors are infinite and the turned-on resistors are zero. For 2-stage MPVD, there are four

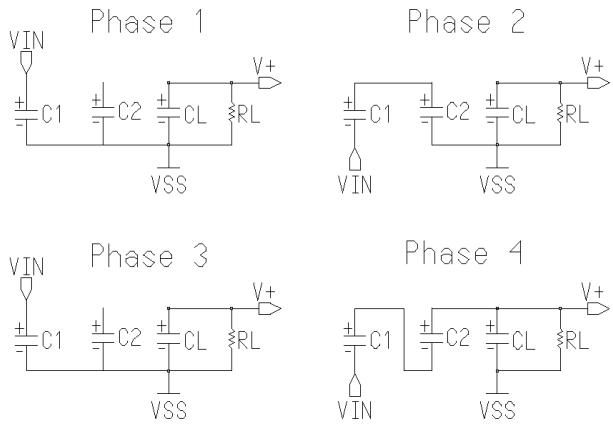

Fig. 7. Equivalent circuits of 2-stage MPVD

phases, the equivalent circuit for each phase is shown in Fig. 7.

In an ideal condition, by assuming C1 = C2 = C and the periods CK1 and CK2 equal to T, the average output voltage V+ is given by:

$$\overline{V}+ = \frac{4 \times VIN}{1 + \frac{3T}{2C \times RL} + \frac{3T}{8C \times RL}} \qquad (1)$$

The output voltage is affected by the load resistor. When there is no load (RL $\rightarrow \infty$) the V+ equals to 4*VIN, and with the RL decrease the voltage output goes down.

B. Clock Pairs Generator

Fig. 8 shows a block diagram of the clock pairs generator. It contains a T flip-flop (TFF), a non-overlapping clock pairs converter, and several level shifters and buffer circuits. The TFF is used to get CLOCK2, which has half the frequency of CLOCK.

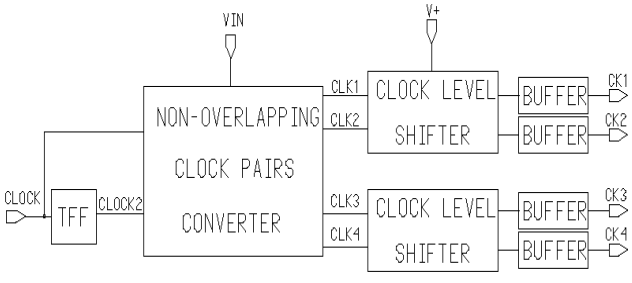

Fig. 8. Clock pairs generator

As shown in Fig. 6, the CK1 and CK2 control the switches of the large transistors. Ideally, if the CK1 is exactly the inverse of CK2, and there is no delay in switching the transistors, the M1 and M2 are not turned-on at the same time. Since the W/L ratios of the transistors are very large (6000/2 for PMOS and 3000/2 for NMOS), the transistors' rise and fall times are very large. Subsequently, it takes a long time to turn these large transistors on and off. To avoid the situation in which both M1 and M2 enter the transition state, the clock pair CK1 and CK2 must be designed to guarantee that before M1 is turned on, M2 must be turned off completely, and vice versa. To make sure that there is no short circuit current, and considering that a mismatch may occur during fabrication, the off-time (both CK1 and CK2 are turned off) should be several times larger than the rise time plus the fall time of the large transistors.

The schematic of the non-overlapping clock generator is shown in Fig. 9. The generated clock pair CK1 and CK2 with their inverse clock pair CKN1 and CKN2 are non-overlapping.

The RC-INV shown in Fig. 10 is used to achieve

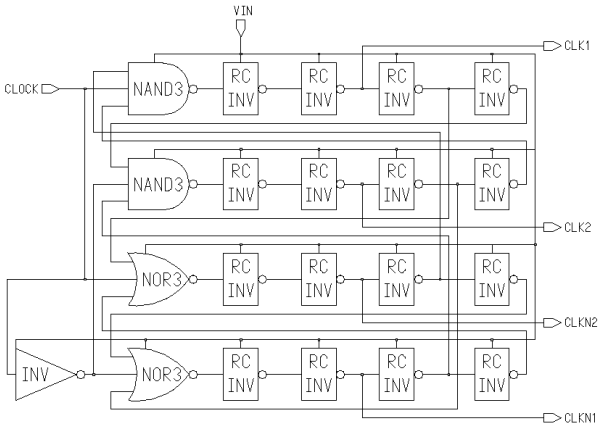

Fig. 9. Non-overlapping clock pairs converter

the required delay. M1 is a PMOS transistor whose gate is connected to VIN, and it is kept in the turned-on state to work as a resistor. M2 is an NMOS that acts as a capacitor. These two transistors control the required RC delay. The right two transistors (M3 and M4) act as the CMOS inverter. The RC-INV behaves as an inverter with long rise and fall time.

The simulation results of the non-overlapping clock generator reveal that the output clock pairs have the same period (50us) as the input clock. The off-time is about 600ns. Compared to the clock period, the off-time is very small and does not affect the clock characteristic. The off-time is much larger than the rise and fall time of the large transistors (about 50ns) to avoid the short current during switching.

As mentioned earlier, the substrates of all PMOS transistors are connected to V+. To turn these MOS transistors on and off properly, the controlling clock pairs should have the amplitude of V+. A clock level shifter is designed to shift the clock level, and its schematic is shown in Fig. 11. Simulation results show that the CKO has the same phase as CK and CKO has amplitude V+.

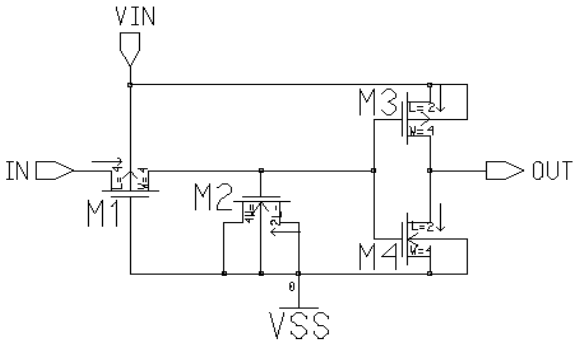

Fig. 10. RC-inverter

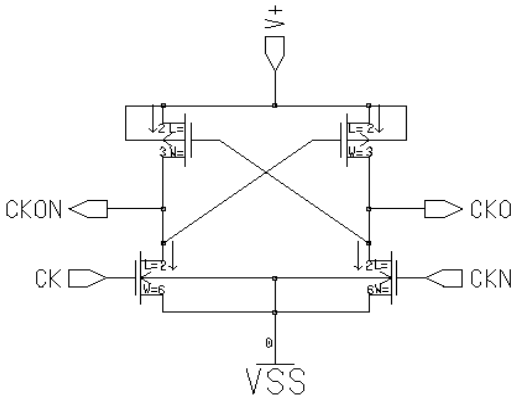

Fig. 11. Clock level shifter

The rise time and the fall time of these 8 large transistors are very large. It will take a long time if the clock pair drives these transistors directly, there is a risk of a short current during switching, even for 600 ns off-time for the non-overlapping clock pair. To reduce the time spent in turning these transistors on and off, the driving buffers are designed.

As discussed earlier, the controlling clock pairs work with V+ as logic 1 and VSS as logic 0 by using the clock level shifter. However, when the MPVD starts to pump, the initial value of V+ is 0V, and after shifting the clock to the initial level, the switching circuit does not work. To avoid this condition, a diode is used to force the initial value for V+. When V+ is charged to be larger than VIN, the diode has the reverse polarization and no energy is dissipated through the diode.

C. Pumping Efficiency

We have discussed the 2-stage MPVD under an ideal condition. In a practical implementation, there is a power loss in delivering the charge from the power source to the load resistor. The power loss contains two components -- resistive and dynamic power losses. The resistive power loss occurs when the current goes through the large transistors, and most of the dynamic power loss occurs as a result of switching the large transistors. Some of the power loss transfers to heat that can harm the integrated circuit. Since both conductive and dynamic power losses reduce the power efficiency, it is important to reduce the power loss to a minimum value for a desired output power.

To reduce the resistive power loss, the most obvious way is to reduce the turn-on resistor's values. The turned-on resistors can be reduced by choosing the large ratio of W/L, thus reducing the resistor power loss.

There are two main components of the dynamic power losses in this switching circuit. One is the power loss in charging and discharging the MOS gates, the other is the loss in diffusion capacitors of the source-bulk and the drain-bulk pn-junctions. Since the controlling clock pairs CK1 and CK2 have the clock period T, and CK3 and CK4 have the clock period 2T, (all of them with amplitude V+), the switching power loss in gate capacitors P_g is given by:

Let us check the source-bulk and the drain-bulk pn-junction of the MPVD as shown in Fig. 6. Every large

$$P_g = \frac{C_{ox}V+^2}{T}\sum_{i=1}^{4} W_i L_i + \frac{C_{ox}V+^2}{2T}\sum_{j=5}^{8} W_j L_j \qquad (2)$$

transistor has one terminal (source or drain) kept at a constant voltage with the other terminal having a voltage level shifted during switching. These voltage level varying pn-junctions behave as capacitors and cause the dynamic power loss described by:

Where $C_{PD/S}$ is the drain/source capacitance of PMOS, and $C_{ND/S}$ is that of NMOS. The dynamic power

$$P_{D/S} = (9C_{PD/S} + 3C_{ND/S})VIN / T \qquad (3)$$

loss is the sum of P_g and $P_{D/S}$ and depends on the frequency and the value of W and L of the large transistors.

To get the higher pumping efficiency, both resistive and dynamic power loss should be reduced. As discussed earlier, the ratio of W/L should be large to reduce resistive power loss, and the product W*L should be small to reduce the dynamic power. First, L is set to the minimum size of 2.0 μm required by SCN Orbits design rule, then W can be designed to minimize $P_g + P_{D/S}$. The optimized W equals to 3000 μm for NMOS and 6000 μm for PMOS.

When the load becomes lighter, with less charge consumed in RL, the current through transistors decreases, which reduces the resistive power loss. The factors affecting the dynamic power loss do not change. Since the power output is decreased due to the lighter load, the ratio of the power loss over the power output increases, which reduces the pumping efficiency. Especially for the no load condition, the charge pump still wastes a large amount of power, and the power

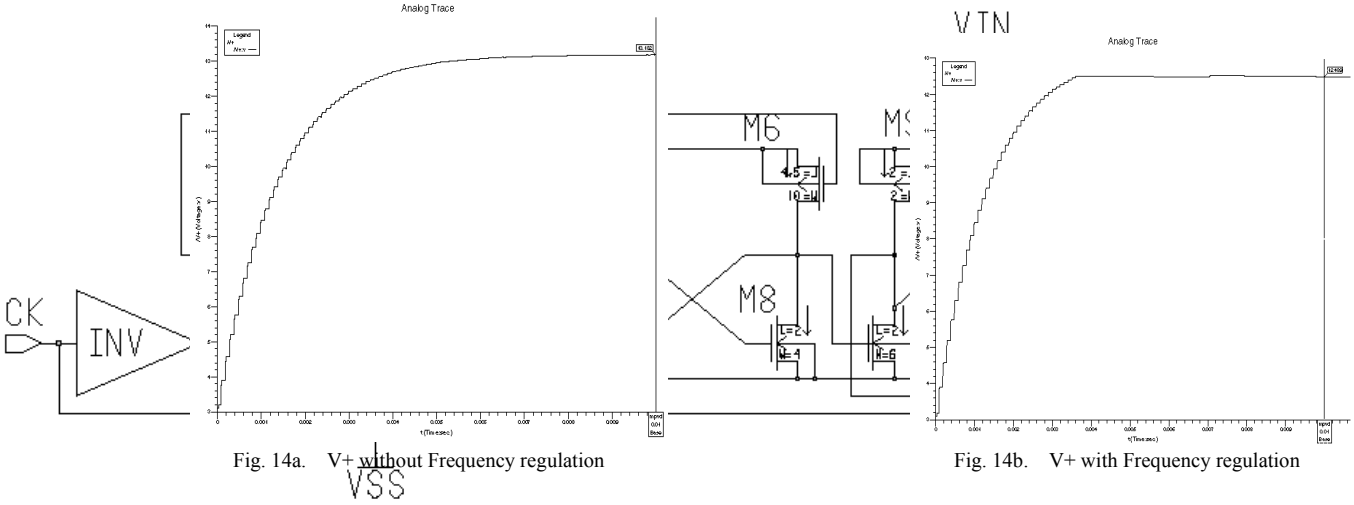

Fig. 14a. V+ without Frequency regulation

Fig. 14b. V+ with Frequency regulation

Fig. 12. Frequency regulator

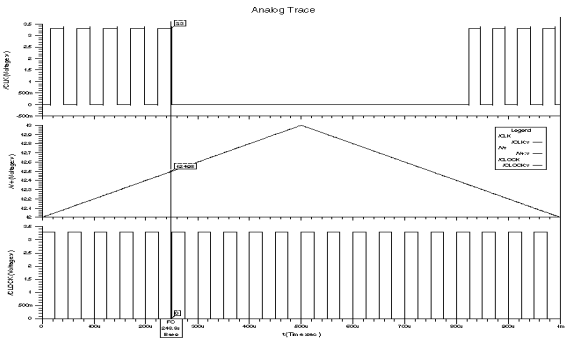

Fig. 13. Simulation result of frequency regulator

efficiency is 0%. To avoid this situation the frequency must be lowered, which is discussed in the next section.

IV. FREQUENCY REGULATION

The frequency regulator shown in Fig. 12 is used to improve the pumping efficiency when the load becomes light.

This circuit has 12 transistors. The left part (left four transistors) is the core of the circuit, and is used to convert the frequency and shift the voltage level of the clock to V+. The middle part (middle four transistors) is designed to keep the clock characteristic much sharper. The right part (right four transistors) is used to shift the level of the clock back to obtain the amplitude VIN.

This circuit has two stable states. We define the time taken from one state changing to the other as response time. If half of the clock period T of CK is longer than the response time, the circuit is varying in these two states. Otherwise, the circuit has no time to respond and will stay in one stable state.

The ratios of the 12 transistors are selected to make the response time close to 25us when V+ is 12.5V. Simulation results reveal that a higher V+ results in a longer response time. As shown in Fig. 13, the output CLK is delayed compared to the input CK. When V+ reaches 12.48V the CLK stops changing, and when V+ changes back to 12.39V, CLK starts to change again.

By adding the frequency regulator to the 2-stage MPVD, the MPVD starts charging with a delay of the frequency regulator which is less than 25us. If the load is light enough to let V+ reach a voltage higher than 12.5V, then the controlling clock pairs stops, and V+ does not increase any more. To drive the load and to cover the power loss in the circuit, V+ drops below 12.5V, which restarts the switching, therefore, this charge pump works in a lower frequency and reduces the dynamic power loss.

V. SIMULATION RESULTS AND CONCLUSION

Fig. 14 shows the simulation of V+ under no load. Fig. 14a shows the result without frequency regulation. After 200 clock periods, the output voltage reaches 13.182V, and is 3.995 times as large as power supply 3.3V. Fig. 14b displays the result with frequency regulation. After 73 clock periods, the output voltage reaches 12.49V, then stays at this level with a deviation of ±0.15V.The period of the controlling clock pair CK1 and CK2 is converted from 20kHz to about 100Hz.

Table 1 shows the simulation results of the 2-stage MPVD with different load resistors. Pin represents the Power supplied by VIN and Pout is the Power consumed in load resistor RL. The upper part shows the result without frequency regulation, in which the V+ goes down with the decreasing load resistors, and when the load is 500Ω, and the output voltage can only reach 5.11V. When the load is about 1KΩ, the power output driving ability is at its maximum value 56.2mW, but the power efficiency is only 41.9%. This huge power loss

can harm the integrated circuit during switching. The maximum power efficiency (84.6%) occurs when the load resistor is 5KΩ, where the MPVD works at a heavier or lighter load than 5KΩ, the power efficiency is lower.

The lower part of Table 1 shows the results with frequency regulation. When the load resistor is no more than 5kΩ, the results are almost identical to those of the upper part. This means the frequency regulator does not affect the circuit performance. When the load becomes light, the output voltage stays at 12.50V, resulting in the power output being a little lower than that of upper part. Nevertheless, the power efficiency is dramatically improved. When there is no load, even the power efficiency is 0%, but the input power is 0.083mW, while without a frequency regulator it is 1.85mW. This reduces the power loss by a factor 22. We can also see from Table 1, that a steady voltage output of 12.5V is obtained when the load is no more than 10kΩ. A stable level of the output voltage with different load values is another advantage of the frequency regulation used.

Table 1. Simulation results of V+ and power efficiency with different load resistors

MPVD without frequency regulation				
RL(Ohm)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency(%)
no load	13.18	1.85	0	0
100K	13.16	3.85	1.73	44.9
50K	13.11	5.32	3.44	64.7
20K	12.92	10.5	8.36	79.6
10K	12.55	18.9	15.8	83.6
5K	11.87	33.7	28.5	84.6
2K	9.75	73.2	47.9	65.4
1K	7.46	134	56.2	41.9
500	5.11	255	53.3	20.9
MPVD with frequency regulation				
RL(Ohm)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency (%)
no load	12.5	0.083	0	0
100K	12.5	1.75	1.56	89.1
50K	12.5	3.43	3.13	91.3
20K	12.5	8.46	7.81	92.3
10K	12.5	17.2	15.6	90.7
5K	11.87	33.7	28.3	84.0
2K	9.75	73.5	47.6	64.8
1K	7.46	134	56.1	41.9
500	5.11	255	53.3	20.9

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