Low-Power Tuneable Analog Circuit Blocks Based on Nanoscale Dual-Gate MOSFETs

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***Abstract*—We illustrate unique examples of low-power tunable analog circuits built using independently driven nano-scale DG-MOSFETs, where the top gate response is altered by application of a control voltage on the bottom gate. In particular, we provide examples for a single-ended CMOS amplifier pair, a Schmitt Trigger circuit and a OTA-C filter, circuit blocks essential for low-noise high-performance integrated circuits for analog applications. The topologies and biasing schemes explored here show how the nanoscale DG-MOSFETs may pave way for efficient, tolerant and smaller circuits with tunable characteristics.**

Keywords-DG-MOSFET; Low-power Analog Circuits; Tunable Analog Circuits; Mixed-mode simulations; DGMOSFET

I. INTRODUCTION

In the final stretch of CMOS down-scaling trend, projected to reach 22 nm limit by 2010 [1], dual-gate (DG) MOSFET architectures on SOI substrates are expected to replace the traditional bulk device structures [2,3]. While multi-gate SOI structures are ideal for digital performance, they will be also strong contenders for analogue RF applications in lucrative wireless communications market due to their ability to effectively handle GHz modulation, to minimize parasitics via low-loss substrate and to cross-modulate dual gates through thin silicon body. However, the actual potential of DG-MOSFETs have not been assessed in detail and there is a clear gap in the literature with regards to analog circuit applications. Hence, it is imperative to explore this gap, surveying and exploiting unique features of DG-MOSFET's especially for specific RF signal processing tasks [4,5].

A particularly attractive possibility for analog circuit applications is the tunability of DG-MOSFETs' front gate functionality via bottom gate bias [6,7]. This has a number of important implications for circuit design: i) increased functionality out of a given set of devices; and ii) reduction of parasitics and layout area, iii) higher-speed operation and low-power consumption with respect to equivalent conventional circuits. Although several works that utilizes DG-MOSFETs in RF mixing applications have been published so far [6-8], the tunability of the DG-MOSFETs have been largely ignored by the analog designers. In the present paper, we will explore several simple analog circuit blocks built using DG-MOSFETs, in which bottom gate is used to tune circuit performance. We will show how compact low-power circuits

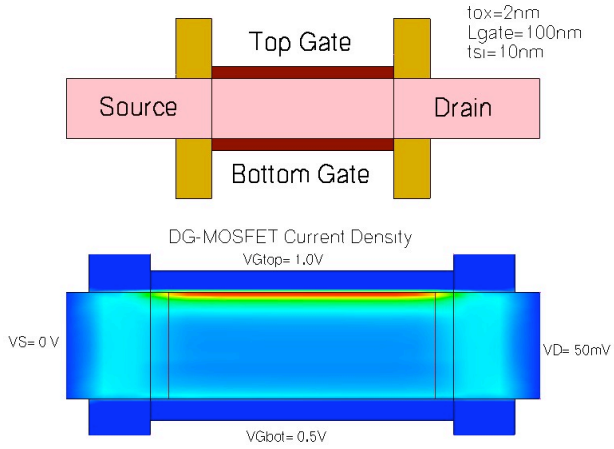

Figure 1. The DG-MOSFET device structure (top) used in this work has a gate length L_g=100nm, a body thickness t_{Si}=10nm and oxide thickness t_{Ox}=2nm, which reflect typical values for those digital applications. DESSIS device simulator is used in mixed-mode simulation mode this simulations and Drift-Diffusion approximation is employed to reduce the computaional cost. Current density distribution at an asymmetric bias condition is shown above, where the top channel is fully on.

including single-ended amplifiers, Schmitt Trigger blocks and differential operational transconductance amplifiers (OTA) may be built and tuned using TCAD simulations. Thus we attempt to provide valuable insight into novel analog design strategies and circuits based on DG-MOSFETs optimized normally for digital applications.

II. DEVICE STRUCTURE AND MODELING

DG-MOSFETs considered in this work are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with minimal overhead to the fabrication sequence. This implies using DG-MOSFETs with a minimal body thickness ($t_{Si}\leq$30nm), oxide insulator thickness ($t_{ox}\leq$5nm) and gate length ($L\leq$100nm), and maximum I_{ON}/I_{OFF} ratio optimized normally for minimum switching delay•power product [9]. It is also assumed that both gates have been optimized for symmetrical threshold $V_T=\pm$0.25V using a dual-metal process. A generic DG-MOSFET structure based on these design guidelines and in agreement with the experimentally demonstrated devices is given in Fig.1a. 2D simulations of this structure are

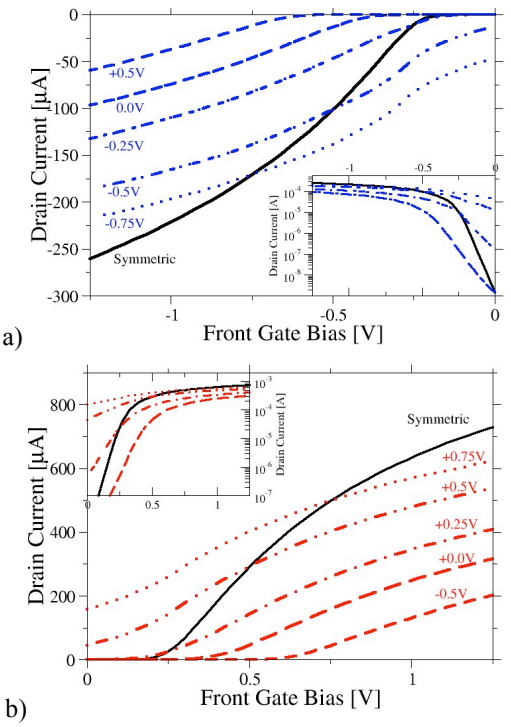

Figure 2. Simulated characteristics of DG-MOSFETs used in this work. For both the (a) pMOSFET and (b) nMOSFETs, we provide I_D-V_{Gtop} plots for different back gate bias conditions labelled. For comparison symmetric (V_{bg}=V_{fg}) drive condition is also included in the plots. Insets show the same data in the semi-log scale, which reveal the well-known deterioration of subthreshold slope in asymmetrically driven DG-MOSFETs

accomplished using DESSIS [10] in drift-diffusion approximation for carrier transport, which is sufficient for low-power circuit-configurations explored here. Fig.1b shows a typical current-density distribution in an asymmetrically biased n-type DG-MOSFET, where the higher bias of top-gate induces a more conductive channel.

With the device structure fixed, we can tailor analog performance by the use of bottom-gate bias. This is best illustrated in Figs.2a&b, where the drain current through *n*- and *p*-type DG-MOSFETs driven from top-gate is studied as a function of bottom gate bias. While the threshold of individual DG-MOSFETs can be modified using this approach, it must be pointed out that the resulting independently driven devices (IDDG, Fig.3a) are always inferior to symmetrically driven counterparts (SDDG) in terms of transconductance and sub-threshold performance, under equal geometry and bias conditions. Thus bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by variety of circuit possibilities, as explored below.

III. Simple CMOS Amplifier

The DG CMOS inverter pair (see Fig.3b) constitutes one of the simplest yet most important design blocks also for analog circuit engineering. When biased in the transition region, it can serve as a high-gain push-pull amplifier. Depending on the selection of the sign and magnitude of the

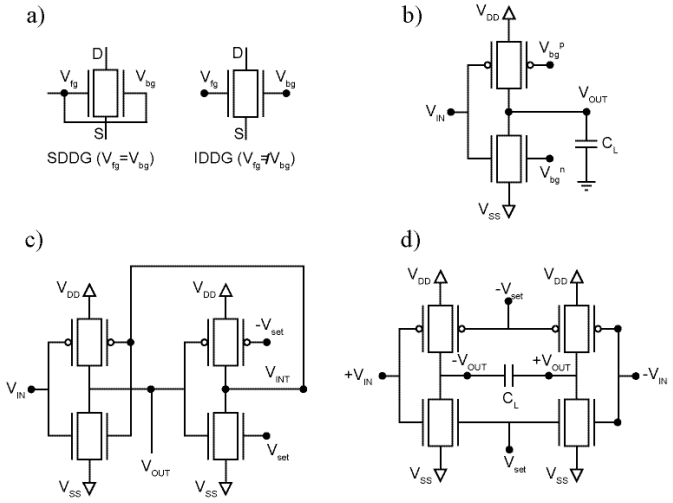

Figure 3. DG bias conventions SDDG and IDDG refers to *symetrically* and *independently* driven dual-gates, respectively. The main analog circuit blocks considered in this work incorporates a) a simple CMOS analog amplifier, b) a Schmitt trigger and c) an OTA-C integrator in which various IDDG configurations are employed to tune main performance metrics, namely gain-bandwidth, hysteresis and transconductance.

bottom-gate bias, the simple amplifier's characteristics can be altered in a number of ways, which greatly enhances the variety of applications for this otherwise simple circuit.

Fig.4 shows that the setting of the CMOS pairs' bottom gates at the same voltage (V_{bg}^n= V_{bg}^p) results in proportional shifts in the voltage window for amplification. This "window-shifting" can be conveniently utilized in a number of ways: in analog wave-shaping circuits sensitive to DC bias levels or in Schmitt triggers (see below). Please note that the amount of shift in this circuit is dictated by the strength of the capacitive coupling via the bottom-gate, which can be adjusted easily by the choice of gate insulator thickness, dielectric constant or the body thickness in a given technology.

An alternative scheme for programming the CMOS pair is conjugation, whereby the two complementary bottom-gates are driven by separate signals of equal magnitude but opposite polarity, i.e. $V_{bg}^n = -V_{bg}^p$. In a mixed-mode design using bipolar supply voltages, this biasing scheme is indeed possible and provides a method of varying the amplifier gain that may be highly desirable. As shown in Fig.5, the slope (gain) of the transition region is a function of conjugate bias levels set on the bottom gates. In principle, it should be possible to change the gain arbitrarily by application of an appropriate level of conjugate bias, whereas we have limited ourselves in Fig.5 to ±0.5V, the bipolar supply voltages used in the low-power design.

For comparison, we also provide in Fig.4 and Fig.5 the output of SDDG CMOS pair. While the gain of this particular configuration is higher, without any bias control, it offers neither design latitude nor alternative configurations. A similar problem occurs with the self-feedback arrangement included also in Fig.5. In this case the *output* of the IDDG CMOS pair drives their bottom-gates i.e. $V_{bg}^n = V_{bg}^p = V_{OUT}$, which results in a very linear amplifier albeit with a significantly lower gain.

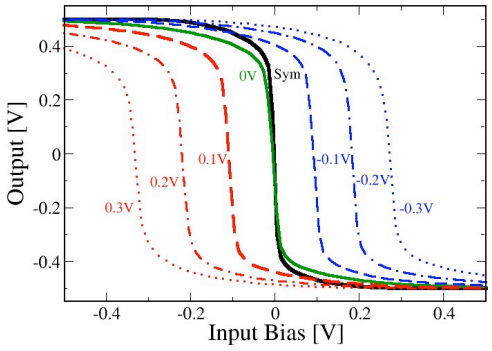

Figure 4. Response of tunable DG-CMOS pair to the setting of same control voltage on the bottom gates ($V_{bg}^{n}= V_{bg}^{p}$). While the amplifier gain remains the same the amplification window shifts proportional to the applied control bias

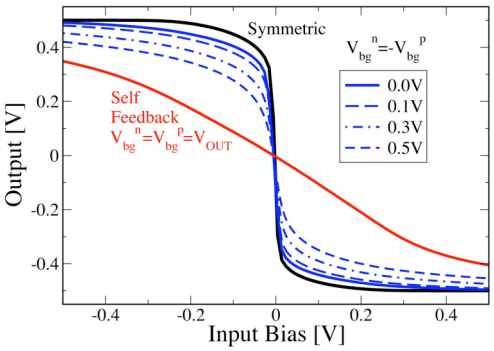

Figure 5 Response of tunable DG-CMOS pair to the conjugate setting of the control voltage on the bottom gates ($V_{bg}^{n}= -V_{bg}^{p}$). This time the amplifier gain changes (lowered) with the applied control bias

This may be especially suitable in applications with stringent linearity requirements that cannot be served with other configurations. It also provides a direct insight into the linearity-gain tradeoff not as well appreciated as the gain-bandwidth tradeoff in analog systems [11]. Such a gain-bandwidth tradeoff is readily illustrated in Fig.6, which shows the outcome of AC analysis performed on the conjugate programming of the IDDG CMOS amplifier driving a load capacitor of C_L=1pF. The linear drop in the gain versus an increase in the bandwidth is well resolved in these simulations performed as a function of conjugate control setting. Thus it should be possible to fine tune simple CMOS amplifier's frequency response using the conjugate biasing scheme.

IV. SCHMITT TRIGGER

The ability to laterally shift the CMOS amplifier's transfer response paves the way for the construction of a simple Schmitt Trigger circuit, a non-linear analog block. The possibility of a DG Schmitt trigger is especially interesting for several reasons: i) leads to a reduction in both area and power usage, ii) can also be used in static memory applications in digital circuits, iii) shows that significant leverage of device functionality is possible when feedback is included.

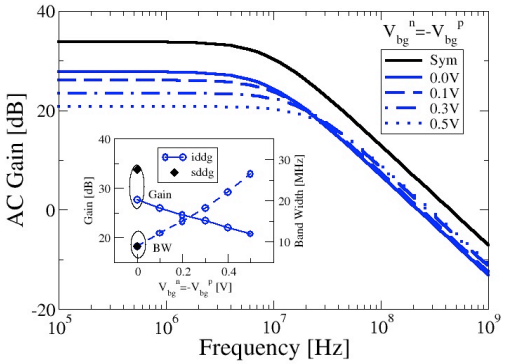

Figure 6. AC analysis of DG CMOS amplifier pair driven with conjugate back gate bias. The inset shows the gain-bandwidth tradeoff for this simple single-ended amplifier extracted from the main plot.

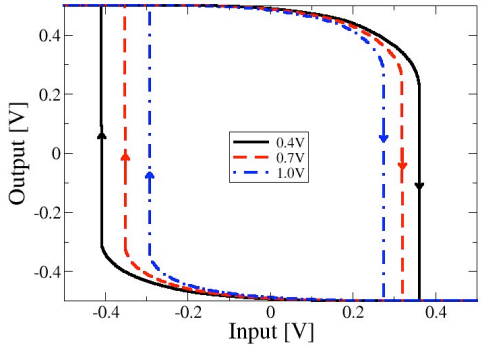

Figure 7. Simulated DC response of a tunable Schmitt Trigger built using only 4 DG-MOSFETs (Fig.3c). Note that large hystereses may be obtained with relatively large programming voltages thanks to large gain of CMOS pair used in the second stage for feedback

In our design, we use only four DG-MOSFETs as opposed to 6 MOSFETs needed in bulk CMOS design [12]. While a similar design was announced before, no programmability was illustrated previously [12]. As indicated in Fig.3c, we consider a two-stage circuit with the conjugate programming of the second stage used to shift the first stage's response on the input plane to two opposite extremes. The simulated output of the Schmitt Trigger circuit is shown in Fig.7 for three different bias settings. Note that between the up- and down-sweep cases output makes transitions at different thresholds, as expected.

The conjugate bias conditions required to set the two extremes, i.e. the width of the hysteresis, can be decided from Fig.4. Because of the relatively large gain of the second stage, very large hysteresis widths can be achieved easily. To design a small hysteresis there are two options: either application of a relatively large conjugate bias or use of self-feedback circuit (see Fig.5) in the second stage. However, the latter has no programming latitude and results in a fixed hysteresis curves. Yet another way of optimizing the Schmitt Trigger circuits would be to reduce bottom-gate coupling by a thicker gate oxide, which would result in smaller shifts in Fig.4 between bias settings. This requires process changes and may be a less desirable path than voltage tuning, which can be realized in a number of alternative fashions besides the above approach.

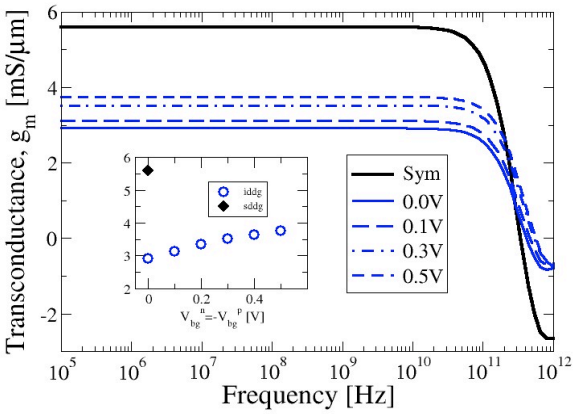

Figure 8. AC performance of differential OTA circuit (C_L=0), given in Fig.3d, as a function of conjugate tuning bias across the two CMOS pairs.

V. Operational Transconductance Amplifier - OTA

OTA's produce differential output currents in response to differential voltage inputs. They have become increasingly popular in the last two decades due to ease of design and reduction in circuit complexity compared to operational voltage amplifiers [13] in specific applications. They often drive a capacitive load in a compact OTA-C block that can act as very efficient integrators and appear also in other filter elements. Fig.3d illustrates a simple OTA structure adapted from conventional MOS circuits which normally requires 6 transistors [14]. The availability of the individual bottom gates allows the elimination of the two extra transistors for transconductance (g_m) tuning across the two branches of the OTA, which saves both power and area.

Fig.8 summarizes the dependence of the AC performance of an OTA-C integrator on conjugate programming voltage for the case of C_L=0pF, i.e. only parasitic overlap capacitances load the circuit. The most important figure of merit, g_m, of OTA varies linearly with programming voltage and the bandwidth of the integrator is constant despite varying g_m, which is one of the main reasons for the use of OTA [13].

VI. Conclusion

Unique and novel examples of low-power analog circuit blocks based on DG-MOSFETs have been investigated. Using mixed-mode TCAD simulations, we have shown how the bottom-gate of an independently driven DG-MOSFETs may be used to design and test analog circuits with tunable performance metrics. In particular, we have provided examples for a simple CMOS amplifier pair, a Schmitt Trigger circuit and an OTA-C filter. In all cases, the main figures of merit, the gain, the hysteresis and the transconductance, respectively, can be varied by application of a specific bottom-gate bias conditions that provide local changes in CMOS pair response. The circuits and biasing schemes explored here show how the nanoscale DG-MOSFETs may pave way for efficient, tolerant and smaller circuits with tunable characteristics.

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