Noninvasive Voltage Measurement Through an On-chip Test Structure

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Abstract

A method to evaluate internal voltages through a built-in test structure is presented. Multiplexers are used to increase accessibility. The test structure does not affect normal operation of the circuit. Individual subcircuits can be tested selectively based on evaluated internal voltages.

Introduction

Testing of integrated circuits is important in circuit fabrication and maintenance. However, testing of large scale circuits is both difficult and costly. It is difficult to directly access internal nodes for functional testing and costly to analyze test results for fault locations [1]. A method needs to be developed to perform reliable testing of large scale circuits with minimal cost and complexity.

Analog circuit fault diagnosis based on sensitivity computation and functional testing [2,3,4] or based on element modulation [5] have been studied over the years. These approaches can be applied to linear and nonlinear circuit testing. Modeling of analog and mixed-signal circuits is also very important [6,7]. Decomposition techniques, which can be used for testing of large analog and mixed mode circuits, were presented in [8,9]. Voltage measurements at the partition points were used to reduce an effect of a faulty element to a localized area. Measurements in digitized form are stored in the waveform recorder for further processing by computerized test equipment. The decomposition technique allows separation of digital and analog parts, and therefore testing (parameter identification) can be performed on each part separately.

Voltage measurements of internal nodes of large scale circuits are important in circuit modeling, simulation and diagnosis processes. However, it is impractical to take voltage measurements inside the chip. First, there is no direct access to internal nodes. Second, a probe placed on an integrated circuit can damage MOS transistors. Hence the development of an internal voltage measurement technique becomes critical for integrated circuit (IC) testing.

To facilitate testing of the IC chip, design may include an additional circuit such as a multiplexer, and a shift register. This design methodology, commonly used in digital circuits, would also benefit analog circuits or mixed-signal circuits testing [10]. In this paper, a method of evaluating the internal voltages based on an external voltage measurement through a built-in test structure is presented. The test structure, however, will not interfere with normal operation of the circuit being tested. If it is desirable to access more than one node, a multiplexer may be used. A multiplexer with m control lines can access 2^m internal nodes. A multiplexer minimizes the number of pins used. Voltages inside an analog or a mixed-signal circuit are evaluated by solving MOSFET i-v characteristics equations. We first illustrate our technique with a simple test structure. This is followed by a discussion of a practical implementation of the method. Two circuits are used to illustrate the method.

Basic Concept

Our aim is to determine the voltage of the selected test point inside an analog (or mixed-mode) circuit. This voltage can be used in device modeling, functional testing, fault diagnosis, and parameter identification. We wish to obtain this voltage without interfering with normal circuit operation.

The basic test structure in Figure 1 consists of three MOSFET transistors, a test transistor M_1, a pass transistor M_2, a charge control transistor M_3, and an external capacitor C_{ex}. The gate of the n-channel MOSFET M_1 (node 1), is connected to the desired node to be evaluated. Node 3 is connected to the designated test pin where the actual voltage measurements are made. The pass transistor M_2 is controlled by the external control pulse signal P which switches between normal operation mode and testing mode. During normal circuit operation, M_2 is turned off by sending a low pulse signal P. The external capacitor C_{ex} will not affect normal circuit operation. Before testing, C_{ex} is charged to V_{dd} through the p-channel MOS M_3. During testing, M_2 is turned on by sending a high pulse signal P. The charges stored in the capacitor C_{ex} are then discharged through M_2 and M_1. The voltage across the capacitor V_c is measured and the discharge current can be determined by the following equation:

$$I_c = C_{ex} \frac{d V_c}{d t} . \qquad (1)$$

The capacitor C_{ex} is used in order to avoid current measurements, since these are more difficult to obtain than voltage measurements. If an accurate current measurement can be made, C_{ex} and M_3 could be omitted from the test structure. In such a case, we would apply an external voltage source to node 3 and measure the current flowing through the source.

If the voltage being evaluated at the desired node is less than the threshold voltage, M_1 would be off. To ensure that M_1 is turned on, a negative bias voltage is applied to the source of M_1 so that $V_{gl} > V_{t0}$ at all times.

The discharged current is related to the voltage at the desired internal node (gate of M_1, node 1) through the following equation.

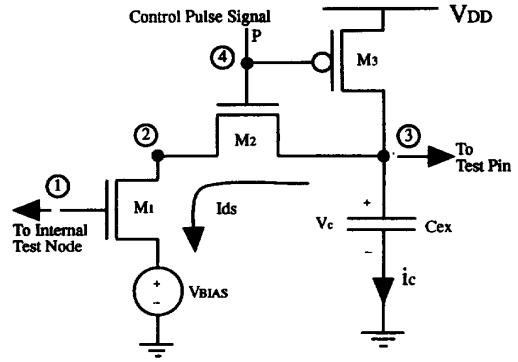

Figure 1. Basic test structure.

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In the linear region where $V_{gs} - V_t > V_{ds}$, the drain to source current is

$$I_{ds} = K \left[V_{gs} - V_t - \frac{V_{ds}}{2}\right] V_{ds} \quad (2)$$

and in the saturated region where $0 < V_{gs} - V_t < V_{ds}$

$$I_{ds} = \frac{K}{2} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}), \quad (3)$$

where

$$K = k_p \frac{W}{L - 2X_{ld}} = \frac{\epsilon \mu}{D} \frac{W}{L - 2X_{ld}} \quad (4)$$

k_p is the transconductance coefficient, ϵ is the oxide permittivity , μ is the mobility of electrons or holes, W is the channel width, L is the channel length, D is the oxide thickness, X_{ld} is the lateral diffusion, λ is the channel-length modulation, and V_t stands for the threshold voltage of the MOS transistor. The threshold voltage is adjusted to consider the effect of the body to source potential V_{bs}

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_p - V_{bs}} - \sqrt{2\phi_p}) \quad (5)$$

where γ is the bulk threshold parameter, $2\phi_p$ the surface potential, V_{bs} is the voltage between the body and source, and V_{t0} is the threshold voltage when $V_{bs} = 0$.

After measuring the voltage at the test node (node 3), V_{g1} is evaluated using the following steps:

Step 1. Evaluate the drain-source currents of M_1 and M_2.

During testing (M_2 is switched on), the charged capacitor C_{ex} is discharged through M_1 and M_2. The discharge current I_c is determined from equation (1). Since the charge control transistor M_3 is turned off during testing, the discharge current I_c is equal to the current flowing through the transistors M_1 and M_2,

$$I_{ds} = I_{d1} = I_{d2} = -I_c . \quad (6)$$

Step 2. Evaluate the drain-source voltage of M_2.

For simplicity, we keep the MOSFET M_2 operating in the linear region. A control pulse signal V_P is selected such that $V_P - V_{t2} > V_c$ to ensure M_2 is in the linear region. The threshold voltage V_{t2} will increase due to the body effect, as V_{bs2} increases. Taking this into consideration, we substitute equation (5) into the linear region i-v characteristic (2) yielding

$$I_{ds} = K[V_{gs2} - V_{t0} - \gamma(\sqrt{2\phi_p - V_{bs2}} - \sqrt{2\phi_p}) - \frac{V_{ds2}}{2}] V_{ds2} \quad (7)$$

After manipulating, the equation can be expressed as a function of V_{s2} as follows:

$$F(V_s) = I_{ds} - K[V_{g2} - \frac{V_{s2}}{2} - V_{t0} - \frac{V_{d2}}{2} - \gamma(\sqrt{2\phi_p - V_{b2} - V_{s2}} - \sqrt{2\phi_p})] (V_{d2} - V_{s2}) (1 + \lambda V_{d2} - \lambda V_{s2}) \quad (8)$$

The only unknown in this equation is V_{s2}, the voltage at the source of M_2 or the voltage at node 2. We can solve this equation to obtain V_{s2} using the Newton Raphson method.

Step 3. Calculate the gate-source of M_1

To evaluate V_{gs1}, we have to determine if MOSFET M_1 is in the linear or saturation region. First we compute I_{dss}, the drain to source current on the boundary between the linear and saturation regions. Using (3)

$$I_{dss} = \frac{K}{2} V_{ds1}^2 (1 + \lambda V_{ds1}) \quad (9)$$

where

$$V_{ds1} = V_{s2} - V_{bias} \quad (10)$$

If $I_{ds} > I_{dss}$, M_1 is in its linear region and V_{gs1} is evaluated by solving equation (2) for transistor M_1. We have

$$V_{gs1} = \frac{I_{ds}}{K V_{ds1}} + \frac{V_{ds1}}{2} + V_{t1} \quad (11)$$

If $I_{ds} < I_{dss}$, then the transistor M_1 is in its saturation region and V_{gs1} is obtained by solving equation (3). We get

$$V_{gs1} = \sqrt{\frac{2 I_{ds}}{K (1 + \lambda V_{ds1})}} + V_{t1} . \quad (12)$$

where V_{t1} is the threshold voltage after considering the body effect. If a bias voltage is used at the source of M_1, the voltage at the desired node can be obtained by the following equation

$$V_{g1} = V_{gs1} + V_{bias} \quad (13)$$

In summary, the voltage being evaluated is calculated using the following algorithm.

Algorithm 1

1. Evaluate the discharge current I_{ds} based on the measured voltage V_c using (1).
2. Evaluate the source voltage of M_2, V_{s2}, by solving nonlinear equation of (8) using the Newton-Raphson method. The body effect due to V_{bs2} is taken into the consideration in the equation.
3. Evaluate the gate-source voltage of M_1, V_{gs1}, by solving equations (11) or (12) depending on the operating region of the transistor. If a bias voltage exists, the gate voltage of M_1, V_{g1}, is recalculated using equation (13).

The important feature of the method is that the test can be conducted without any interference with normal circuit operation. The only alteration in the original signal path is a slight increase of the line capacitance (several nanofarads) due to the insertion of the test structure M_1. However, this increase in the line capacitance is negligible in many analog circuits. Even in circuits where the added gate capacitance of the test structure is comparable with the load line capacitance, it can be accounted for during the design stage.

Practical Implementation

Due to the limited number of input/output pins, we can use a multiplexer instead of a single pass transistor to increase the accessibility. With m control lines, we can access 2^m internal nodes as shown in Figure 2.

A 1-to-4 multiplexer test structure shown in Figure 3 is used as an example. Node v is connected to the test pin at which actual voltage measurement are taken during testing.

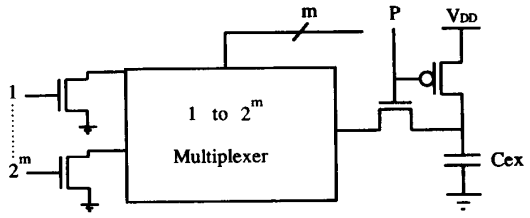

Figure 2. Implementation of test structure.

To minimize pin usage, V_{dd} is the highest potential applied to A and B. ($\overline{A}$ and $\overline{B}$ are the outputs of CMOS inverters, with a high voltage of V_{dd}.) The pass transistor must be designed to have a voltage drop, V_{ds}, sufficiently high to ensure that the transistors of the multiplexer operate in the linear region. One of four internal nodes can be accessed at a time depending on the signals at A and B. For example, when A and B are both high, the voltage at the node 1 can be evaluated through the path v–w–x–y–z using the following algorithm.

Algorithm 2

1. Evaluate the discharge current I_{ds} based on the measured voltage V_c using (1).
2. Evaluate the voltages at w, x, and *y* by solving the corresponding nonlinear equation (8).
3. Evaluate the voltage at z, (voltage at the node 1), by solving equations (11) or (12) depending on the operating region of the transistor. If bias voltage exists, v_z is adjusted using (13).

The voltages at nodes 2 , 3 and 4 can be evaluated using the same algorithm.

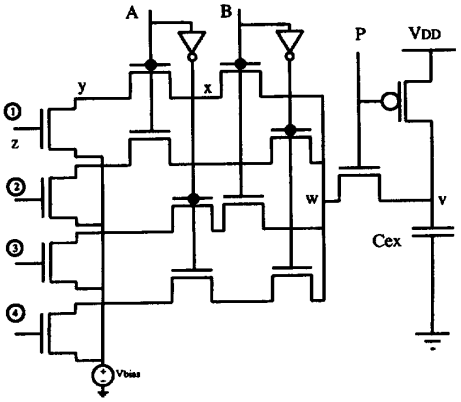

Figure 8. 1-to-4 Multiplexer test structure.

Computer Results

To illustrate this method, two circuits, an inverter and an operational amplifier (OpAmp) are tested. The basic test structure is used to evaluate the output of the inverter, and the 1–to–4 multiplexer test structure is used to evaluate voltages at four internal nodes of the OpAmp.

The circuits were designed using Magic layout tools, distributed by the University of California at Berkeley. The extracted netlist files were simulated using Pspice, the product of MicroSim Corp.. Algorithms were programmed in Fortran and analyses run on Sun SPARCstation 2 at Lafayette College.

Example 1: Basic Test Structure and Inverter.

The test structure is connected to the output of the inverter as shown in Figure 4. The Pspice simulation is shown in Figure 5. A square pulse is applied to the input of the inverter. An external pulse signal V(P) is applied to the pass transistor to switch between operation mode (V(P) is low) and test mode (V(P) is high). The external capacitor C_{ex} is charged to V_{dd} when V(P) is low and discharged when V(P) turns high. During testing, the voltage across the external capacitor C_{ex}, $V(C_{ex})$, is measured and used to evaluate the output voltage, which is connected to the basic test structure. The output waveform is calculated using Algorithm 1. The actual output (simulated by Pspice) and calculated output are plotted in Figure 6. The maximum error in the plot is less than 0.1 volt.

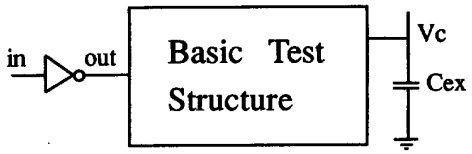

Figure 4. Test circuit 1 - An inverter.

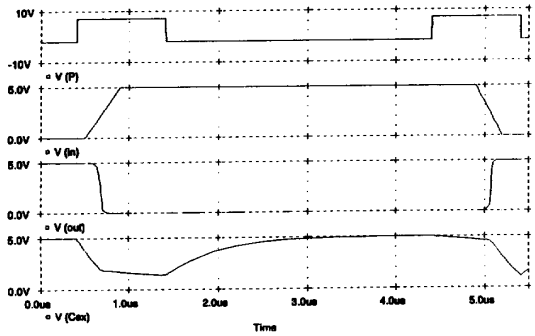

Figure 5. Pspice simulation results of test circuit 1.

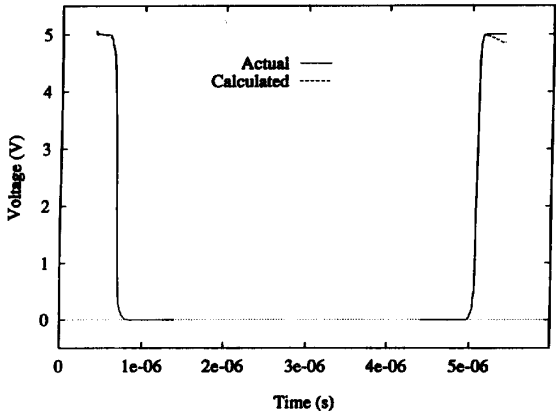

Figure 6. Actual and calculated output waveforms of the inverter.

Example 2: 1–to–4 Multiplexer test structure and OpAmp.

An operational amplifier circuit shown in Figure 7 was designed and used in the inverting configuration shown in Figure 8 to perform the test. The 1–to–4 multiplexer test structure was connected to the Opamp to evaluate the voltages at the internal nodes 1, 2, 3, and 4. The voltages at nodes 1, 2, 3, and 4 are evaluated at different time intervals depending on the control signals A and B. The voltages are calculated using Algorithm 2 four times successively. The actual waveforms obtained through Pspice simulation and the calculated waveforms are plotted in Figure 9. The maximum error is less than 0.5 volt.

Another experiment was to evaluate different waveforms using the multiplexer test structure. A sinewave signal, exponential function, a rising transition and a falling transition were evaluated at nodes 1, 2, 3, and 4, respectively. Algorithm 2 was used to calculate these waveforms and the results are plotted in the Figure 10. The maximum error is less than 0.4 volt.

Simulation results demonstrate the feasibility of evaluating internal voltages based on external measurements. For higher precision, the i–v characteristic equations of MOSFET (level 2,3 or 4) can be considered.

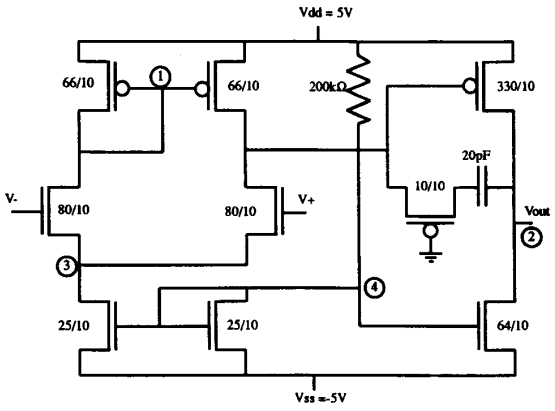

Figure 7. Test circuit 2 - An operational amplifier.

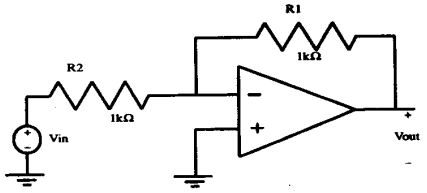

Figure 8. Inverting configuration of the Opamp.

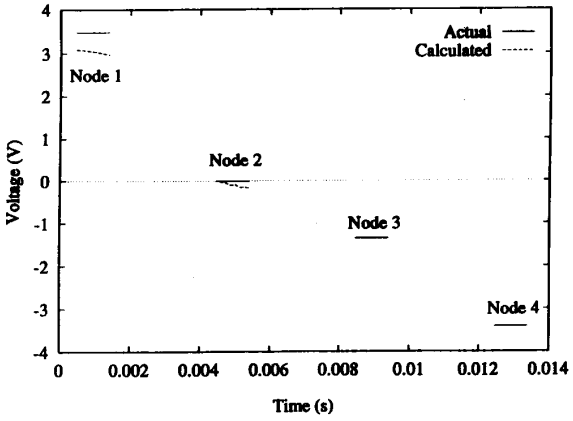

Figure 9. Actual and calculated waveforms of the Opamp.

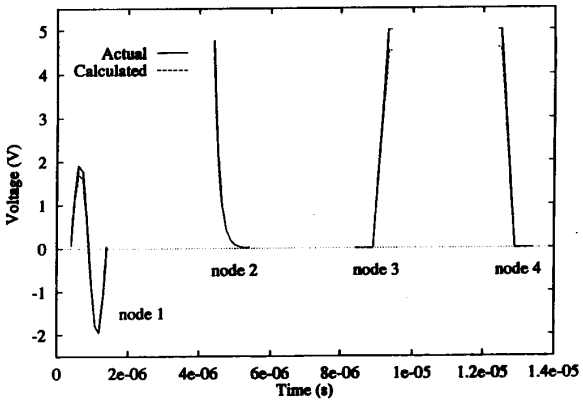

Figure 10. Actual and calculated waveforms.

Other noninvasive test structures can be developed using the principle of voltage measurements, through the observation of the current charges on the output of the test structure. The requirements for such structures are twofold:

(1) The structure should not be a significant load to the tested circuit.

(2) It should have a monotonically increasing (preferably linear) voltage current transfer function.

Such structures are currently being investigated.

Conclusions

To facilitate analog and mixed-signal testing, designs may include a test structure such as those proposed in this paper. Using the multiplexer test structure, internal nodes of the circuit can be accessed, thus increasing system observability. In that case, digital subcircuits are tested using algorithms for digital testing while analog subcircuits are tested as discussed in [2,3,4]. In a complex system, different subnetworks can be simulated and tested using different circuit representation levels. Some sub-networks may be tested on the functional or macromodel level for functional testing, while others may be tested on the element level for element identification. When the circuit is nonlinear, the circuit can be decomposed into linear and nonlinear parts and each of these parts tested separately.

Many modern VLSI digital circuits incorporate a significant amount of analog circuitry. The test method developed here can be used to test custom integrated circuits such as analog/digital converters, filters, voltage regulators or operational amplifiers. It can be also applied to test VLSI neural networks or complicated mixed mode circuits.

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