An Organization of the Test Bus for Analog and Mixed-Signal Systems

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ABSTRACT

System level solutions for error detection in analog and mixed-signal circuits are presented in this paper. Internal blocks of an analog circuit are accessed using a technique similar to the boundary scan organization. Test points are controlled by a digital control signal scanned into a system, and the test signal and test results are connected to an analog test bus. Analog response can be verified either on-line without interruption to the signal path, or in a test mode. No new elements (like virtual or real switches) are added to the signal path. As a result the proposed test bus can be easily incorporated in the existing designs as an add-on feature enhancing system testability.

I. Introduction

Design for test (DFT) reduces time-to-market by saving prototype debug and reducing production test set-up. It also contributes to savings in the field service. A DFT philosophy known as the boundary-scan design (BSD) has been accepted throughout electronic industry and is implemented as IEEE standard P1149.1 [1] for digital circuits. Using BSD, a designer can incorporate the latest PCB design with the microchip modules (MCM), surface mounted devices (SMDs), and IC packages, which include complex ASICs, RISC microprocessors, and DSP chips. While testing of digital circuits has been facilitated by IEEE P1149.1 standard, testing of analog and mixed-signal networks remains a major problem. As the complexity of analog and mixed-signal circuits increased, the need for automatic tests of these circuits became critical. In this paper, a new analog test bus compatible with the proposed IEEE P1149.4 [2] standard is discussed to facilitate analog and mixed-signal testing.

Built-in testing structures may be used to access test points only or to perform test as well. In the former case, the tested circuit response is fed to the external tester for evaluation. In the later case, the response is evaluated internally using built-in self testing (BIST) circuit. An internal BIST circuit can work in the test only mode, in which it evaluates the circuit response to the internally generated stimulus, or in the observe only mode in which it performs on-line testing.

In the paper we describe general organization of analog test bus, the analog boundary scan cell structure, and the operating modes. This paper is divided into 5 parts. Section II describes the concept of the analog test bus. Section III describes the structure of the analog boundary scan cell. The simulation results are presented in Section IV. Finally, the conclusion is given in Section V.

II. Concept of the analog test bus

Two basic concepts of the boundary scan approach are circuit partitioning and test signal scanning. The implementation of circuit partitioning in analog circuits is the leading topic of discussions of the Working Group for the IEEE P1149.4 mixed-signal

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test bus standard. However, there are fundamental differences between analog and digital testing, which make duplication of the solutions satisfactory for digital testing difficult to adopt for analog testing. When a digital switch is inserted into the signal path of a digital circuit to enforce circuit partitioning, its effect can be tolerated. In the worst case, an extra clock delay is needed. In an analog circuit, insertion of a switch into the signal path may cause a major deformation of the signal itself, which must be corrected at the design stage.

Scanning is also more difficult in analog systems than in digital. First, there is no reliable analog memory or shift register cells which can be used in high speed applications. Second, any distortion of the analog signal along the interconnection lines may have a significant effect on the test results.

An attempt to implement test signal scanning was made [3], but a practical implementation of this approach is limited. First, the analog signal is sampled to be shifted out for evaluation. This limits the bandwidth of the tested signals. Distortions of the analog signal shifted through a chain of the registers will cause inaccuracies in analog signal evaluation. Finally, the proposed scan chain does not have the benefits of the digital scan path, since each analog signal has to be directly shifted out for evaluation through a number of switches. Since the number of switches is different depending on the test point location, signal delays and distortions will depend on the number of switches in the scan path.

An alternative to signal scanning is to either evaluate the tested signal at the test point locations using built-in signal transformation networks and comparators, or to preprocess the analog signal locally, transform the resulting signal to a digital form, and shift it out for evaluation using the boundary scan organization for digital signals.

Three organizations of built-in test circuits for analog designs were presented in [4]. Two of these organizations are very similar . The first one is based on multiplexing test data to and from analog subcircuits. The second organization uses the analog bus and analog transmission gates to access the analog subcircuits. This organization most closely resembles the IEEE P1149.1 standard and is the closest to the IEEE P1194.4 standard currently under consideration. Where the signal delay caused by insertion of the transmission gate into the signal path is unacceptable, an organization similar to the observe-only configuration of the digital boundary scan test should be adopted. The observe-only approach has an advantage over active testing (in which a signal is forced into a tested unit) in systems where a high reliability is required.

The third organization of analog built-in testing presented in [4] uses analog switches to form a scan chain. This approach may be useful for DC testing, where signal delays along the scan chain are not critical for evaluation of the circuit performance. In general, this organization will be limited in a similar way as the BIST structure discussed in [3].

In the boundary scan testing, partitioning of the UUT into smaller circuits is accomplished by inserting the boundary scan cells into the signal path. During test-only mode, the signal path is opened by a switch and the testing signal delivered to the UUT. This solution is adequate for digital testing, where the effect of the boundary scan cell on circuit performance is reduced to a single gate delay. This effect can be easily accommodated at the design stage.

In analog circuits, additional elements placed in the signal path may dramatically change the circuit performance. One can try to modify the design in

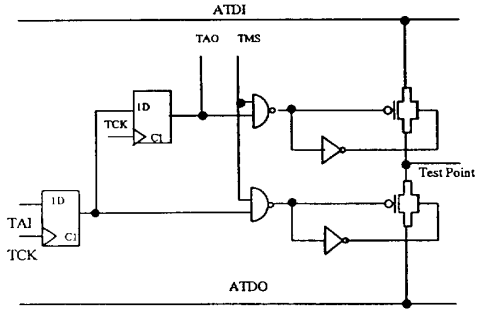

Fig. 1 Analog Boundary Scan Cell.

order to incorporate the analog switches, and produce a modified circuit with so called "virtual switches". However, up to date, there is no systematic design procedure which will guarantee successful implementation of such a strategy. In addition, an analog boundary scan cell, which rely on such a strategy, would no longer be a simple add-on feature as the digital BSCs are, instead they would require a redesign effort. For these reasons, it is difficult to expect a wide acceptance of a standard based on a "virtual switch" concept.

III. Structure of the ABSC

A better approach to observing the analog signal values is to use an analog test bus connected directly to the output of a tested circuit. Such a test bus could be connected to test points through analog switches organized in a similar way to the digital boundary scan cells (BSC). Fig. 1 shows an example realization of the analog boundary scan cell considered in this paper. In order to avoid problems of signal distortion which are caused by placing the analog switches in the signal path, a boundary scan cell without such switches is proposed in this work. The graphical symbol of the analog boundary scan cell (ABSC) used is shown in Fig. 2. This cell is activated in the test mode by the test mode select

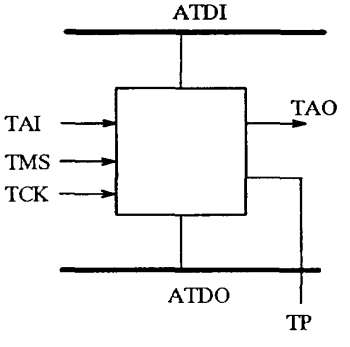

Fig. 2 Symbol of the Analog Boundary Scan Cell.

(TMS) signal. An ABSC connects a selected test point (TP) to the analog bus. The analog bus contains two wires which carry analog test data input (ADI) and analog test data output (ADO) signals. A test point can be connected to either ADI or ADO line by setting a corresponding analog switch inside the ABSC. The switches are controlled by D latches and activated by the TMS signal. Note that the analog switch is placed outside of the normal signal path, and can be combined with a carefully designed testing circuit. In particular the loading effect of the testing circuit can be minimized by connecting a high impedance voltmeter to ADO. If a test signal is to be injected to a test point, the ADI bus is connected to a current source.

If differential signals are to be tested, the output signal may be connected to two different ADO lines

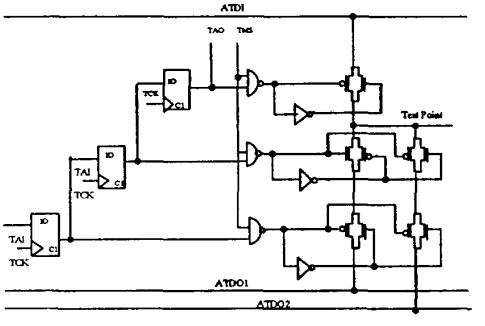

Fig. 3 Modified Analog Boundary Scan Cell.

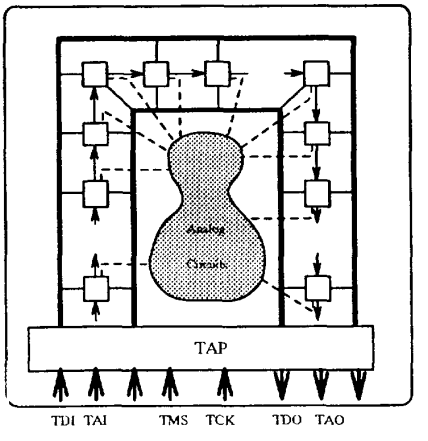

Fig. 4 Chip Level Organization of Analog Test Bus.

as shown in Fig. 3. Individual ABSC's are cascaded and connected to various test points (TP) inside the

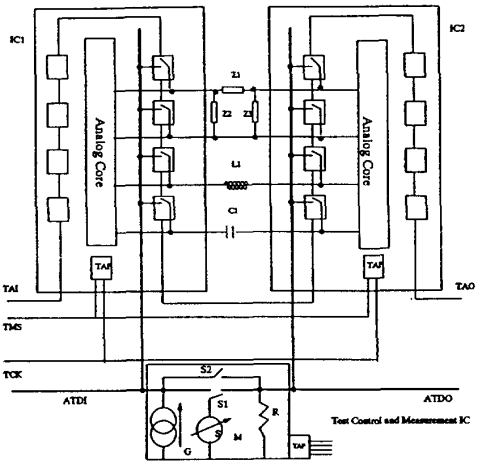

Fig. 5 Testing of Interconnections on a PCB.

analog circuit. In order to select a specific TP, its address is shifted through the sequence of D latches inside the cascaded analog boundary scan cells along TAI and TAO lines. Not only all the input and output pins of analog circuits can be tested using this structure, but all the internal test points, critical to verify the circuit performance, can be tested as well. During the sequential shift operation, test points are disconnected from the analog bus. Chip level organization of analog test bus with its ABSC's is shown in Fig. 4. This structure can be then extended to the board and system levels, in which all chips are scanned sequentially in a fashion similar to the digital boundary scan. Fig. 5 shows the board level organization and the testing of interconnections. Solutions presented on Fig. 5 resembles this of [5] with one exception - there is no change in the signal path between analog parts on the board when testing function is disabled.

IV. Simulation results

Computer simulation of the ABSC was performed using PSPICE simulator. Analog switches are controlled by a signal taken from CMOS buffers

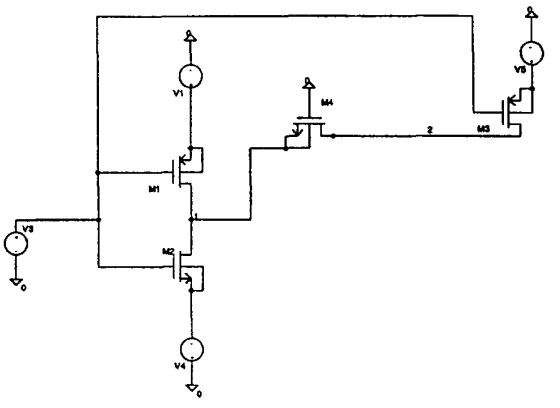

Fig. 6a) D/A CMOS Inverter.

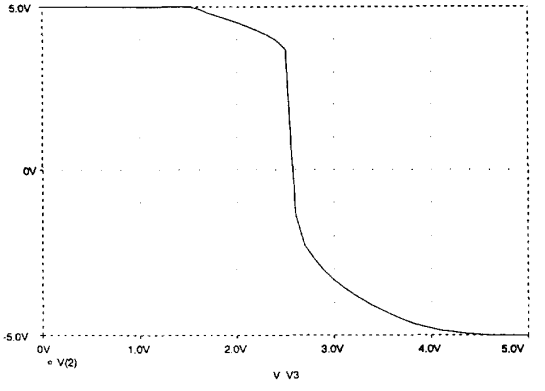

Fig. 6b) Input-Output Characteristic of D/A CMOS Inverter.

which transform digital inputs (with GND and VDD voltage levels) to analog signals within $-V_{max}$, $+V_{max}$ voltage range. The organization of the digital to analog CMOS inverter used in this transformation is shown on Fig. 6a) and its input-output characteristic shown on Fig. 6b). The resistance of the turned-on analog switch changes from 5% to 10% of its average value (500Ω in the test structure) depending on the strength of the tested voltage. The effect of this

variation can be minimized if a high impedance voltmeter is used to measure the output voltage. Fig. 7a) shows the test signal, which is a 20MHz sinewave

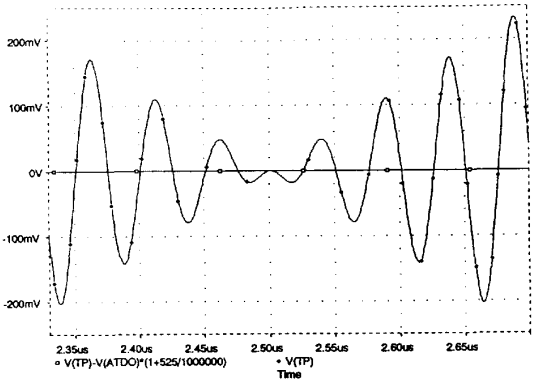

Fig. 7a) The Test Signal.

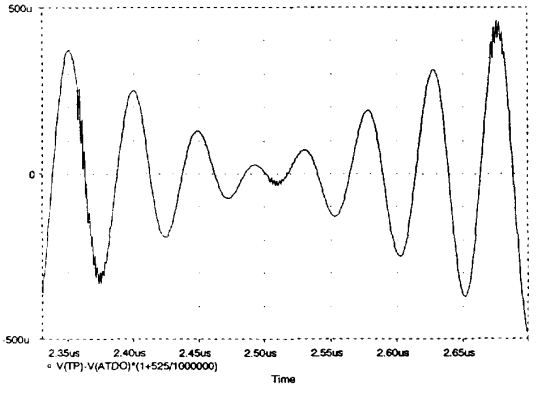

Fig. 7b) The Measured Voltage Error.

modulated by a 200KHz sinewave. Fig. 7b) shows the measured voltage error for the case of a voltmeter with 1MΩ input impedance. This simulation of the ABSC demonstrates that an analog signal can be observed on a selected test point with a precision sufficient not only to check interconnections but to perform an internal test of the analog part as well.

V. Conclusion

In response to the increasing interest in analog and mixed-signal testing, a new analog test bus was proposed and investigated in this paper. Using analog boundary scan cells described in this paper we can decompose circuits into subsystems and access selected test points. In the proposed solution, there is a clear differentiation between analog and digital test points. At the digital test points, the test signals are delivered and the output signals read through the boundary scan cells. However, at the analog test points, test signals are delivered and results are read through the analog test bus. The analog boundary scan cells deliver only the address of the analog test points. The proposed analog test bus may be considered as one more option to investigate before a specific solution is adopted as a mixed-signal test standard.

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