Analog Design Resource Kit Tutorial 1

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CMOS TWO TRANSISTOR INVERTING AMPLIFIERS

Simulation and Measurement

Objective: To simulate and measure the dc transfer characteristic, ac frequency response and amplification properties of a simple two-transistor CMOS inverting amplifier.

Introduction

The simplest inverting CMOS amplifier circuit consists of two FETs, an n-FET pull-down and a p-FET pull-up transistor. This simple configuration has both gates connected together at the input, identical to a CMOS digital inverter, and is shown in Figure 1.

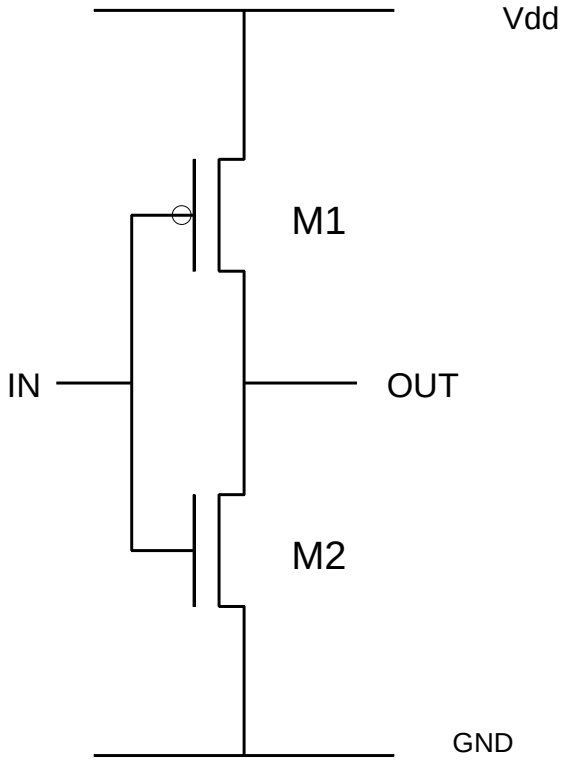


FIGURE 1

The switching characteristic of the CMOS inverter is also the dc transfer characteristic of the inverting amplifier and indicates the dc bias point for biasing the amplifier in the operating region that gives the widest dynamic range and linearity. The approximate input bias voltage calculation assumes that both transistors are operating in their saturation regions and that the amplifier is unloaded [1]. The results of the computation yield an input bias point expression of:

$$V_{IN} = \frac{V_{DD} + V_{TP} + V_{TN}\Delta}{1+\Delta} \tag{1}$$

where

$$\Delta = \frac{\sqrt{K_N (W/L)_N}}{\sqrt{K_P (W/L)_P}}$$

where K_i and (W/L) are the intrinsic transconductance and aspect ratio, respectively, of the appropriate FET.

This same circuit configuration allows both transistors to contribute to the overall circuit transconductance (as well as output conductance). These two factors combine to give the overall unloaded low frequency gain of the circuit, defined by the simple equation given below:

$$A_{Vo} = -\frac{g_{mn} + g_{mp}}{g_{dn} + g_{dp}} \tag{2}$$

where g_{mn} and g_{mp} are the n-FET and p-FET transconductances, respectively and g_{dn} and g_{dp} are the respective drain (or output) conductances. The output impedance of the simple inverting amplifier is simply the denominator of Equation 2; i.e.;

$$r_{out}^{-1} = g_{dn} + g_{dp} \tag{3}$$

The absolute values of A_{Vo} and r_{out} are dependent on the level of dc bias current flowing through the amplifier as well as the aspect ratios of the n-FET and p-FET. The addition of a load capacitor, C_L (such as the output interconnects and output pad capacitance), and load resistor, R_L, causes the output resistance to be the parallel combination of r_{out} and R_L:

$$r_{out}^{'} = r_{out} R_L / (r_{out} + R_L) \tag{4}$$

A load capacitor introduces a single dominant pole into the voltage gain transfer function at frequency:

$$f_{-3dB} = 1/2\pi r_{out}^{'} C_L \tag{5}$$

The laboratory exercises outlined in this tutorial focus on the inverting amplifier subjected to an external load composed of a 100 KΩ resistor and a 50 pF capacitor. These components are external to the on-chip two-transistor inverting amplifier.

The inverting amplifier as-drawn (or drawn during layout) exhibits a p-FET aspect ratio of 95/3 and an n-FET aspect ratio of 47/3 (dimensions are in micrometers). The input and output terminals are both connected directly to an external analog pad that contributes approximately 4 pF of capacitance to each node. The power and ground lines are connected globally. The cell name for the inverting amplifier is **invamp,** as indicated in the CIF file for the chip set. Simulation and measurements on this circuit are described in detail in the following sections.

EQUIPMENT and PINOUT

Equipment

1. Design board with chip set IC
2. Function generator set for sawtooth wave generation
3. Multimeter and/or oscilloscope
4. 5.0 volt power supply (if not included on design board)
5. 47 pF capacitor and 100KΩ Resistor
6. Spectrum/Signal Analyzer (if available)

Important Pins for this experiment

PIN 8 Output of Amplifier 3
PIN 9 Input to Amplifier 3
PIN 10 **Ground**
PIN 11 Output of Amplifier 2
PIN 12 Input to Amplifier 2
PIN 13 Output to Amplifier 1
PIN 14 Input to Amplifier 1
PIN 30 **V_{dd} (+5 volts)**

NOTE: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

DO NOT APPLY SIGNALS TO THE CHIP WITHOUT POWER AND GROUND APPLIED TO THE IC. TO DO SO MAY SET UP UNWANTED LATCH-UP PATHS THAT COULD RESULT IN IMMEDIATE DESTRUCTION OF THE IC!

PROCEDURE

Simulation

1. The first step in testing the inverting amplifier's operation is to simulate the ac and dc response of the amplifier, then compare it with the actual fabricated amplifier's response. Determine the dc transfer function of the inverting amplifiers with aspect ratios listed above. Also determine a value of bias voltage that will bias the inverting amplifier into a region of operation that allows for reasonable gain and output voltage swing. Simulate the dc response using a circuit simulator such as SPICE. An example file showing all the necessary input sources and other command/control statements is presented at the end of the tutorial.

In this command file, the command shown causes a sweep of the input voltage "V_{in}" over the range of 0 to 5 volts in 0.1 volt steps. The input voltage and the results of the dc voltage sweep should be plotted on one graph. Obtain a plot of these responses.

Also determine the ac frequency response of the amplifier from 1 KHz to 10 MHz using SPICE. Use a 10 mV peak input signal and a dc input bias voltage that places the operating point of the amplifier in the linear region (see dc section above).

Measurement

2. This next section describes in-laboratory measurements of the transfer function of the inverting amplifier.

First, adjust the dc power supply for 5.0 volts and verify **before** applying the dc supply to the IC using either a voltmeter or oscilloscope. Connect the power supply to the chip at the appropriate pins (V_{dd} and Ground). Also connect the resistor and capacitor to the output of the inverting amplifier.

Next, prepare an input signal using the function generator. This signal should exhibit the following specifications: a 0 to 5.0 volt 1 KHz sawtooth wave (or, alternately, a triangular wave with low duty cycle). Verify using the oscilloscope that the generator's output is within specifications **before** applying the signal to the appropriate pin.

After verifying that the power supply is energized, apply the ac signal to any one of the amplifiers (they are identical). Observe the output of the amplifier and record the waveform (dc transfer characteristic) displayed on the oscilloscope. If available, use a digital storage oscilloscope to record one of the transfer curves and plot the curve. From the information given in this dc transfer characteristic, select a dc operating point and bias voltage that will bias the amplifier in its high gain and linear region. Estimate the gain of the amplifier from the dc transfer curve.

3. This next set of measurements provides the data to determine the ac frequency response of the amplifier at the dc bias point of your choice. From Section 2, you selected an operating point and bias voltage and determined the gain at the operating point. The next set of measurements is to apply an ac signal at the operating point chosen.

Remove the input ac signal (sawtooth waveform) from the input to the amplifier. Set the function generator so that it will provide a 50 mV signal with the appropriate dc offset (the offset voltage that you determined in Section 2) to the input of the amplifier. Verify using the oscilloscope that the signal is within specifications **before** applying the signal to the IC.

After verifying that the power supply is energized, apply the ac signal to the amplifier you used in Section 2. Vary the frequency from 10 Hz to 10 MHz and observe the frequency response of the amplifier. Record your results and sketch a frequency response plot. (Alternatively, use a spectrum analyzer to measure the frequency response of the amplifier. This requires that a white noise source of appropriate dc offset be applied to the input of the amplifier.)

From your measured 3 dB points, you can estimate the output impedance of the amplifier if you know the capacitance across the amplifier output and assume a single pole response.

QUESTIONS

1. How do the simulated and measured dc transfer curves differ for the two-transistor inverting amplifier? How are they similar? Give quantitative answers.

2. Describe the origin of the off-chip capacitances that you used to determine the total capacitive load on the inverting amplifier.

3. Using the model parameters listed in the SPICE file, determine the theoretical gain and -3dB frequency of the amplifier. How do simplified expressions for these parameters (Equations 2 and 5) compare with the results given by the simulator?

References

1. Weste, N., and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, Reading, MA, p.47, 1988.

SPICE Deck for Simulating the Two Transistor CMOS Inverting Amplifier

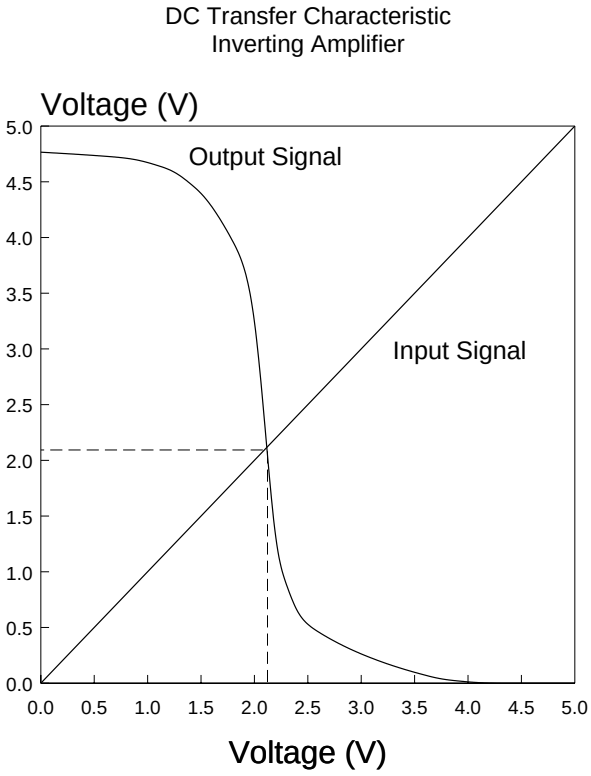
```
*** SPICE DECK created from invamp.sim, tech=scmos
M1 1 4 5 1 CMOSP L=3.0U W=95.0U
M2 5 4 0 0 CMOSN L=3.0U W=47.0U
C3 4 0 0.012000PF
* The following lines show a 50 pF load capacitor in parallel
* with a 100K load resistor.
C4 5 0 50.00000PF
R4 5 0 100K
*  IN      4
*  CMOSN          0
*  CMOSP          1
*  GND  0
*  OUT  5
*  Vdd   1
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
Vdd 1 0 5.0
** To run the specific set of simulations, edit out the appropriate
** section's comment columns (*).
* DC TRANSFER CHARACTERISTIC
* Vin 4 0
* .dc Vin 0 5 0.1
* .plot dc v(4) v(5) (0,6)
* AC TRANSFER CHARACTERISTIC
* Vin 4 0 dc 2.11 ac 0.01
* .ac dec 10 1 1e7
* .plot ac vm(4) vm(5) vp(4) vp(5)
* TRANSIENT ANALYSIS WITH SINUSOIDAL INPUT
* Vin 4 0 sin(2.11 .05 10e3 0 0 0)
* .tran 1u 300u
* .plot tran v(4) v(5)
*  DISTORTION ANALYSIS:  LARGE SIGNAL DISTORTION
* The following "four" line is for those using PSPICE with PROBE Option
*  It performs  a large signal distortion analysis based on a 10 KHz input signal (10e3)
* .four 10e3 v(5)
* The following "probe" line is for those using PSPICE with PROBE Option
* .probe
.end
```

Results of SPICE Simulations

The SPICE file listed in the tutorial contains three different simulations of the two-transistor CMOS inverting amplifier: a dc transfer analysis, an ac frequency response analysis and a transient analysis. The models and components used in these analyses are typical of those used in most measurements. The following set of figures shows the results of each one of the simulations.

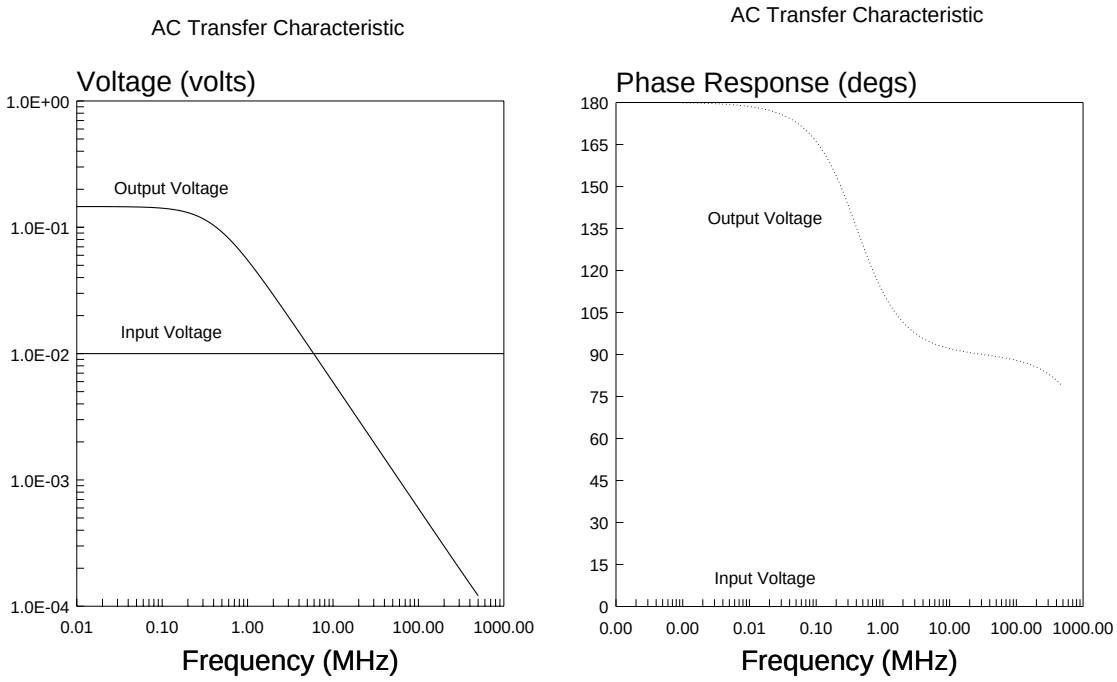
dc Transfer Characteristic

The dc Transfer Characteristic plot shows the input ramp signal [v(4)] and the resulting output signal v(5). The simulated transfer characteristic uses a load of 50 pF in parallel with a 100 KΩ resistor. The figure indicates that an input signal dc offset of approximately 2.1 volts would bias this amplifier in a region that would give about a 2.0 volt swing at the output and still maintain linearity.



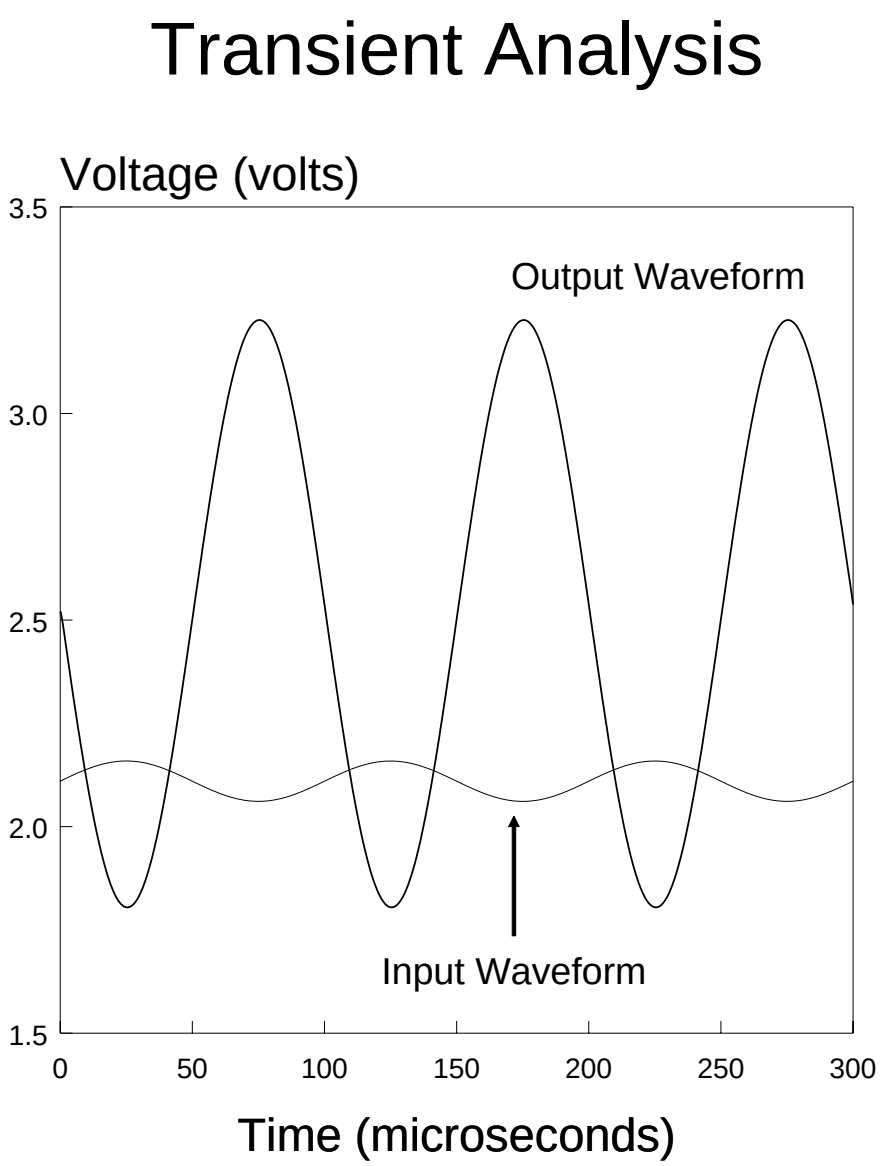
ac Frequency Response

The ac Frequency Response output has been divided into two plots, a magnitude and phase plot. The magnitude plot shows that an input signal of 0.01 volts [vm(4)] yields an output amplitude of approximately 0.15 volts [vm(5)], yielding a low frequency gain magnitude of approximately 15. The -3dB point (gain of 10.65) occurs at a frequency of approximately 500 KHz. The phase plot [vp(5), vp(4)] shows a phase of 3.14 (or π) radians at low frequencies, rolling off to 2.355 (or $3\pi/4$) radians at approximately 500 KHz.



ac Transient Response

The Transient Response shows the amplification properties of the amplifier when excited with a 50 mV, 10 KHz input signal with a 2.1 volt dc offset [v(4)]. The output waveform v(5) shows a 1.4 volt swing for a 0.1 volt input swing, consistent with a gain of -15 (note also the phase inversion between the input signal and output signal). The output waveform appears "clean", but a distortion analysis should be done to determine the extent of any nonlinearities in the output signal.



Fourier Analysis of ac Signal

The ac transient response shows the amplification properties of the amplifier when excited with a 50 mV, 10 KHz input signal with a 2.1 volt dc offset [v(4)]. The output waveform v(5) shows a nearly 1.4 volt swing for a 0.1 volt input swing at the fundamental, but as with any nonlinear device such as a MOSFET, there will be distortion on the signal. The .four command provides distortion information on the output waveform [v(5)] up to the ninth harmonic, and also computes the total harmonic distortion (THD) of the circuit. The 1.4 volt swing is shown in the table for the first harmonic at 10 KHz (6.807E-01 volts peak amplitude). The actual and relative components for the distortion components are indicated in the table. Total harmonic distortion (THD) for the inverting amplifier is also indicated (THD = 0.595%).

FOURIER COMPONENTS OF TRANSIENT RESPONSE v(5)

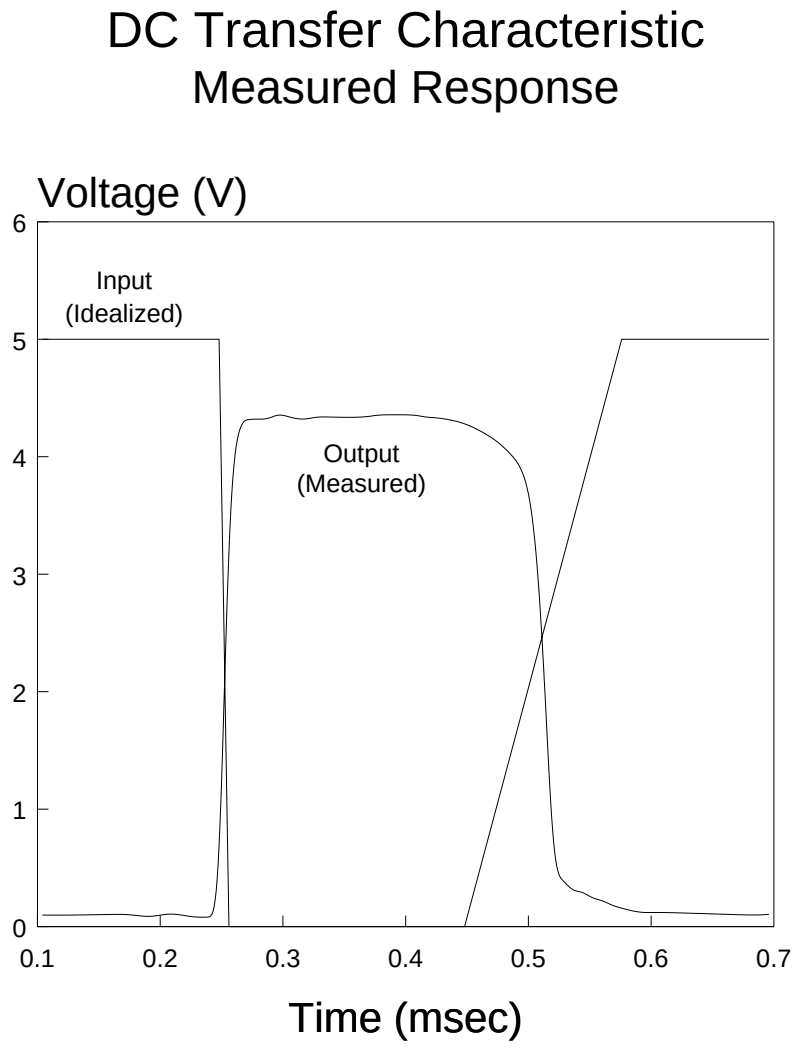
DC COMPONENT = 2.103216E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE PHASE(DEG)	NORMALIZED PHASE(DEG)
1	1.000E+04	6.807E-01	1.000E+00	1.787E+02	0.000E+00
2	2.000E+04	3.936E-04	5.782E-04	-1.300E+02	-3.086E+02
3	3.000E+04	1.724E-03	2.532E-03	-1.139E+02	-2.926E+02
4	4.000E+04	1.633E-03	2.399E-03	-1.129E+02	-2.915E+02
5	5.000E+04	1.591E-03	2.338E-03	-1.186E+02	-2.973E+02
6	6.000E+04	1.530E-03	2.248E-03	-1.239E+02	-3.026E+02
7	7.000E+04	1.462E-03	2.147E-03	-1.292E+02	-3.079E+02
8	8.000E+04	1.385E-03	2.035E-03	-1.342E+02	-3.128E+02
9	9.000E+04	1.305E-03	1.917E-03	-1.391E+02	-3.177E+02

TOTAL HARMONIC DISTORTION = 5.953496E-01 PERCENT

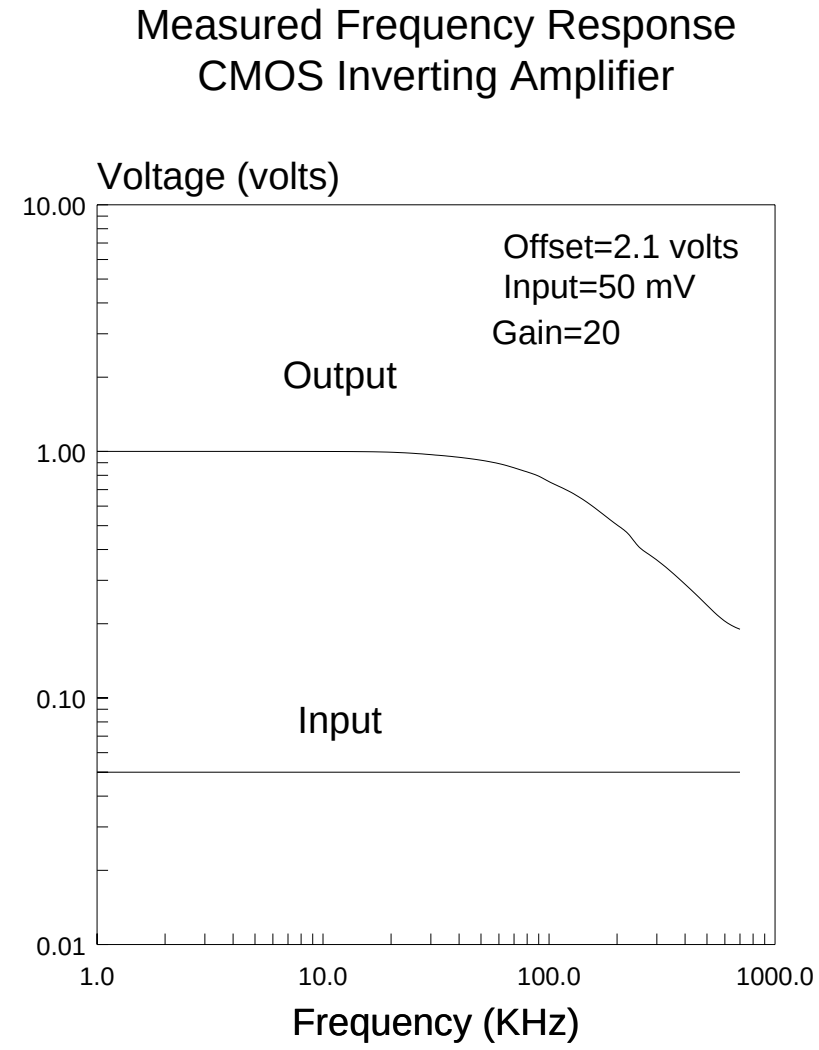
Measured dc Transfer Characteristic

The ac Frequency Response was measured using a 0 to 5 volt triangular waveform with 95% duty cycle. The equipment used for this set of measurements was an HP-3314A function generator and a Tektronix 2230 Digital Storage Oscilloscope. Note the input-output crossover voltage of 2.2 volts, approximately that of the simulation results. The figure below illustrates the measured dc sweep response.



Measured ac Frequency Response

The ac Frequency Response was measured using a 50 mV peak input voltage and a 2.1 volt dc offset. The equipment used for this set of measurements was an HP-3314A function generator and a Tektronix 2230 Digital Storage Oscilloscope. This set of input conditions gave a nominal 1.0 V peak output voltage. The -3dB frequency for the simple inverting amplifier is approximately 120 KHz. The figure below illustrates the measured magnitude response.



Voltage Magnitudes Indicated