Digital Neural Networks in VLSI

Table I.a.

Name	*Architecture*	*Precision*	*Neurons*	*Synapses*	*Learn*	*Avail.*
Nuralogix NLX-420	Multi-layer	1-16b x 1-16b	16	16 offchip	off-chip	commercial
Hecht-Nielson 100 NAP	GP[1], SIMD processors	32b x 32b, FP	100 PE[2]	64	prog.	system
Hitachi WSI	Wafer Scale Net Hopfield	9b x 8b	576	32k	off-chip	research
Inova N64000	GP, SIMD processors	1-16b x 1-16b	64 PE	128k-2M	prog.	system
IBM ZISC036	Radial Basis Functions	8b elements	36 prototypes	64 element prototypes	RCE-like	commercial
MCE MT19003	Multi-layer feedforward	13b x 13b	1 PE	off-chip wts	off-chip	commercial
Micro Devices MD-1220	Multi-layer feedforward	1b x 16b	8	8	off-chip	commercial
Nestor/Intel Ni1000	Radial Basis Functions	5b elements	1024 prototypes	256element prototypes	RCE, PNN	commercial
Philips Lneuro-1	Multi-layer feedforward	1-16b x 1-16b	16 PE offchip TF	16x16	prog.	research
Siemens MA-16	Systolic arry for matrix x matrix	16b x 16b	16 PE offchip TF	64	off-chip	research
RC Module NM6403	Multi-layer feedforward	1-64b x 1-64b	1-64	1-64	prog.	prototypes

[1] **GP** - General purpose architecture
[2] **PE** indicates a processing unit

Table I.b.

Name	*Configuration*	*CPS*[3]	*CPSPW*[4]	*CPPS*[5]	*CUPS*[6]	*Patterns/s*
Nuralogix NLX-420	32-16, 8-bit mode	10M	20k	640M	na	20k
Hecht-Nielson 100 NAP	4-chips, 2M wts, 16bit Mantissa	250M	125	256G	64M	na
Hitachi WSI	576 neuron Hopfield	138M	3,7	9,9G	na	na
Inova N64000	64-64-1, 8bit mode	871M	3.4k, 128k wts	55.7G	220M	100k
IBM ZISC036	64 8bit element input vectors	na	na	na	na	250k
MCE MT19003	4-4-1 at 32MHz clk rate	32M	32M	6.8G	na	140k
Micro Devices MD-1220	8-8	8.9M	1.1M	142M	na	139k
Nestor/Intel Ni1000	256 5bit element input vectors	na	na	na	na	40k
Philips Lneuro-1	1-chip, 8bit mode	26M	26k	1.6G	32M	na
Siemens MA-16	1-chip, 25MHz	400M	15M	103G	na	40k
RC Module NM6403	8bit mode at 50MHz clock rate	1200M	150M	76.8G	na	na

Reference.

C. S. Lindsey, Th. Lindblad, “Survey of Neural Network Hardware”, Proc. SPIE Vol. 2492, p. 1194-1205, Applications and Science of Artificial Neural Networks, Steven K. Rogers; Dennis W. Ruck; Eds. , March 1995.

[3] **CPS** - Connection-Per-Second

[4] **CPSPW** = CPS/Nw, where Nw - number of sinapses per neuron.

[5] **CPPS** - Connection Primitives per Sec, CPPS = CPS*Bw * Bs, were Bw, Bs - word length of weight and sinaps.

[6] **CUPS** - Connection-Update-Per-Second.