O H I O U N I V E R S I T Y

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Introduction to VLSI Systems

Quiz #3

Your Name _____

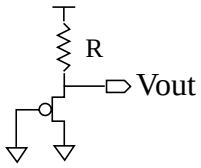
Instructions: This quiz consists of 32 multiple choice questions. Please mark your choices for the best answers on the separate sheet that we have provided, but please hand in **both** the answer sheet and these questions. Please provide a brief explanation to your choices.

You may consult any reference materials you have.

In all figures, unless other wise noted, assume that the body terminal of NFETs are at 0V and the body terminal of PFETs are at VDD.

Questions:

1. In the figure below, assuming that the resistance R is very large, what is the best approximation for Vout?



(A) -Vtp

(B) Vtp

(C) VDD-Vtp

(D) 0

(E) VDD

2. In the figure from the previous question, the body effect makes the voltage Vout:

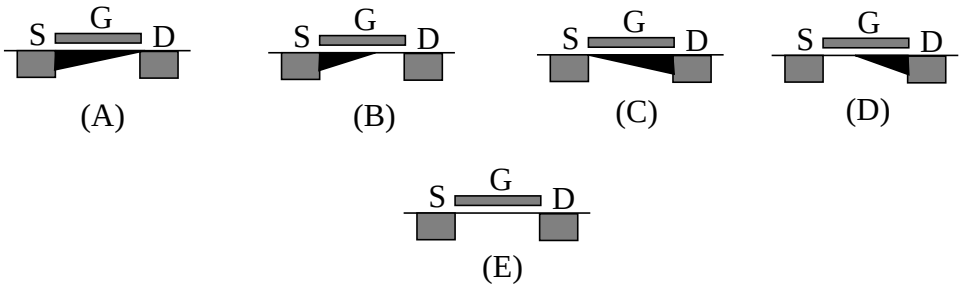
(A) Higher

(B) Lower

(C) No Change

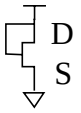
(D) Can’t Tell.

The figures below represent the side view of a MOSFET and its channel in various operating conditions Use these channel diagrams for the next three questions. Assume “typical” digital-process transistors

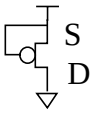


and voltage supplies, i.e., VDD=3V, Vtn=0.7, Vtp=-0.7.

3. Which diagram best represents the channel in the schematic below?

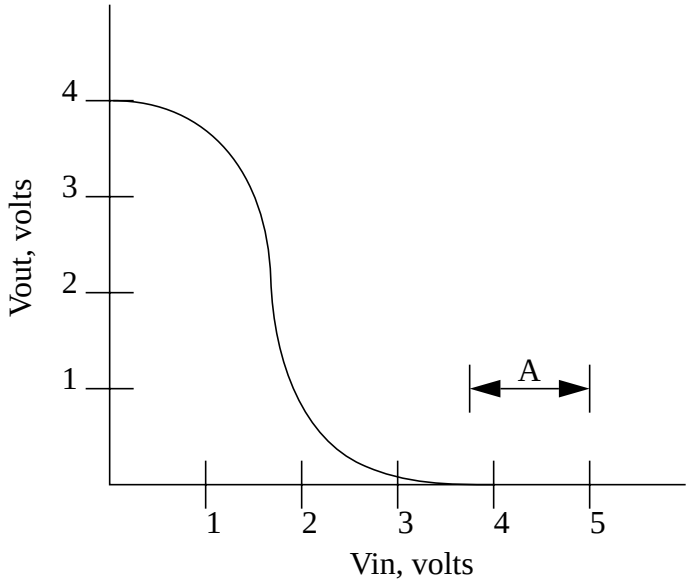


4. Which diagram best represents the channel in the schematic below?



5. Which diagram best represents an NFET with Vgs=3.2V, Vds=3V, Vt=0.7V, and Vsb=0V?

Consider the following voltage transfer curve for a CMOS inverter made from n-channel MOSFETs with a threshold of 1V and from p-channel mosfets with a threshold of -0.5V. Each threshold was measured with Vsb=0 for each MOSFET. Use this figure to answer the next two questions.



6. When the inverter has reached a steady state and is operating in the region marked “A” above, the
   (A) pulldown is in the saturated region, and the pullup is off.
   (B) pulldown is in the linear region, and the pullup is off.
   (C) pulldown is in the linear region, and the pullup is in the linear region.
   (D) pulldown is in the linear region, and the pullup is in the saturated region.
   (E) not enough information to tell.

7. The inverter whose voltage-transfer curve was diagrammed above is being operated with a power supply of

   (A) 4V

   (B) 4V + p-channel threshold = 3.5V

   (C) 4V - p-channel threshold = 4.5V

   (D) need to know Wpu/Wpd

   (E) not enough information to tell.

8. The propagation delay of an inverter was measured using an input with a rise time of 500ps. If the propagation delay of the same inverter were measured using an input with a rise time of 250ps, one would expect the measured delay to be:

   (A) a lot longer (more than 100 ps longer).

   (B) a little longer (10 ps to 100 ps longer).

   (C) about the same (within 10ps of the previous measurement).

   (D) a little shorter (10 ps to 100 ps shorter).

   (E) a lot shorter (more than 100 ps shorter).

9. The powers-that-be have decided to measure the “switching threshold” of an inverter at its Vin=Vout point. A particular inverter is found to have a switching threshold of 2.3V. If the width of the p-channel MOSFET of that inverter were doubled, the new threshold would be:

   (A) lower than 2.3V.

   (B) remain unchanged.

   (C) higher than 2.3V.

   (D) there’s not enough information to say.

   (E) undefined because the device would no longer be an inverter.

10. An inverter driving a 0.5 pF load has fall time of 1.5 ns. The approximate “on” resistance of the n-channel MOSFET is:

    (A) 2 ohms.

    (B) 20 ohms.

    (C) 200 ohms.

    (D) 2000 ohms.

    (E) 20000 ohms.

11. To achieve equal pullup and pulldown times in a CMOS inverter, the P device is usually several times wider than the N device. What is the main reason for this?

    (A) Hole mobility is greater than electron mobility.

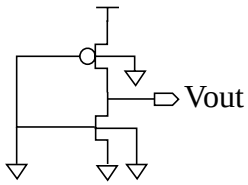
    (B) Electron mobility is greater than hole mobility.

    (C) The P threshold is greater than the N threshold.

    (D) The N threshold is greater than the P threshold.

    (E) None of the above.

12. In the circuit below, what is Vout?



    (A) VDD

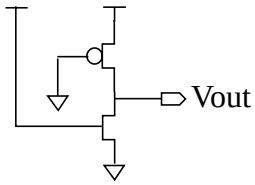
    (B) 0V

    (C) Vtp

    (D) Vtn

    (E) 0.7

13. In the circuit below, what is Vout?



(A) VDD

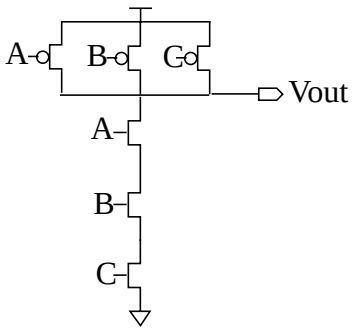
(B) 0V

(C) VDD-Vt

(D) 2.5V

(E) Not enough information to decide.

14. The circuit below



computes what function of A, B, and C?

(A) NAND

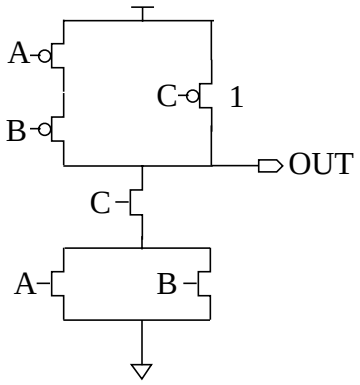
(B) NOR

(C) AND

(D) OR

(E) None of the above.

Use the circuit below to answer the next three questions.



15. Out is what function of A, B, and C?

(A) NOT(C AND (A OR B))

(B) NOT(C OR (A AND B))

(C) (C AND (A OR B))

(D) (C OR (A AND B))

(E) None of the above.

16. If all transistors in the circuit have the same W/L, then, between inputs A and B, which is faster?

    (A) A

    (B) B

    (C) They're the same speed.

    (D) They're different speeds, but can't tell with the information given.

17. For this gate to achieve a rise time no worse than an inverter that has a P device with W/L=3, the transistor number 1 should have a minimum W/L equal to:

    (A) 1.5

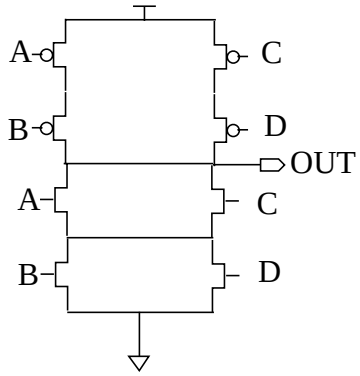
    (B) 3

    (C) 6

    (D) 9

    (E) Can't be determined with information given.

18. What logic function does the following circuit compute?



(A) NOT((A OR B) AND (C OR D))

(B) NOT((A OR C) AND (B OR D))

(C) NOT((A AND B) OR (C AND D))

(D) NOT((A AND C) OR (B AND D))

(E) none of the above, because this is not a static CMOS logic gate.

19. If an “acceptor” type of dopant is added to undoped silicon, the material becomes:

(A) P-type

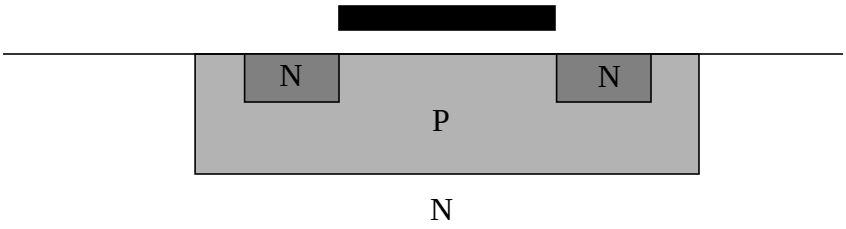
(B) N-type

(C) Source

(D) Drain

(E) Intrinsic

20. The MOSFET below:.



is labelled with the different types of silicon. The device is best described as a:

(A) An NFET in an N-well

(B) An NFET in a P-well

(C) A PFET in an N-well

(D) A PFET in a P-well

21. The primary current carriers in a PFET are:

(A) Electrons

(B) Holes

(C) Boron Ions

(D) Arsenic Ions

(E) Tunnelling Electrons.

22. The Ids current of an NFET with a 0.7V threshold is measured to be 37uA when Vgs=2.6V, Vds=1.2V, and Vsb=0V. If Vsb is raised to 1V, but Vgs and Vds are kept at their previous values, then

    (A) Ids will increase due to channel length modulation.

    (B) Ids will increase due to the body effect.

    (C) Ids will decrease due to channel length modulation.

    (D) Ids will decrease due to the body effect.

    (E) Can't tell what will happen to Ids with the information given.

23. The Ids of a different NFET with a 0.7V threshold voltage is measured to be 50uA when Vgs=2V, Vds=5V, and Vsb=0V. If Vgs increases to 3V, then Ids should go to approximately:

    (A) 75 uA

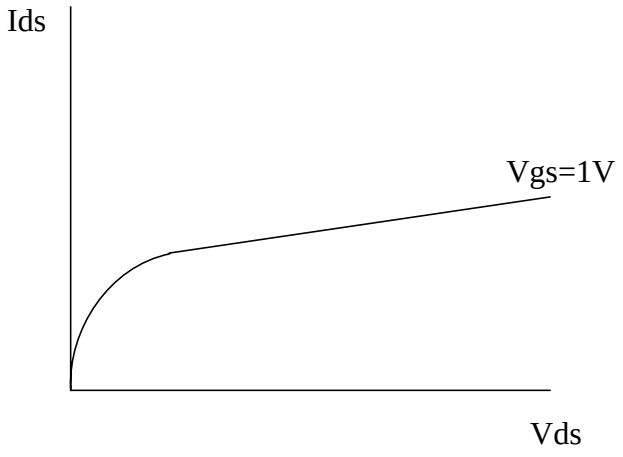
    (B) 100 uA

    (C) 125 uA

    (D) 150 uA

    (E) not enough information to tell.

The figure below shows the relationship between Ids and Vds for an n-channel MOSFET with Vgs=1V.



24. The Ids in the saturation region is not constant, but instead has a slight linear increase. This is due to which second order effect?

    (A) Body effect.

    (B) Fowler-Nordheim Tunneling.

    (C) Electron drift.

    (D) Drain punch through.

    (E) Penfield-Rubenstein approximations.

    (F) none of the above.

25. After a late night out, the fab line technicians accidentally let the thin oxide grow to a much greater thickness than usual. The main effect of this mistake is:

    (A) The Ids of the transistors will be much greater than expected.

    (B) The Ids of the transistors will be much smaller than expected.

    (C) The sheet resistance of the source/drain diffusions will be higher than expected.

    (D) No change will be detected.

    (E) The metal-to-substrate capacitance will be dramatically higher.

26. Suppose that Intel has decided to offer a process-tweaked version of their Pentium processor for laptops that operates with a power supply of 2.5V instead of the usual 3.3V. Assume that the Pentium dissipates no static power, and that both chips operate at the same frequency. Upon receiving this news, customers should:

    (A) expect a reduction in power dissipation to 2.5/3.3 = 75% of the previous level.

    (B) expect a reduction in power dissipation to (2.5*2.5)/(3.3*3.3) = 57% of the previous level.

    (C) call to ask how much capacitance is being switched each cycle before they can estimate the power savings.

    (D) first determine that operating frequency for the Pentium chips before they can estimate the power savings.

    (E) call to ask how much capacitance is being switched *and* determine that operating frequency they plan to run at before they can calculate the power savings (i.e., both C and D).

27. The resistance of a metal1 wire that is 0.6u wide and 600u long is approximately:

(A) 1 ohm

(B) 10 ohms

(C) 100 ohms

(D) 1000 ohms

(E) 10000 ohms

28. Why is polysilicon, rather than metal, used for the gate in modern MOS transistors?

(A) Better channel inversion.

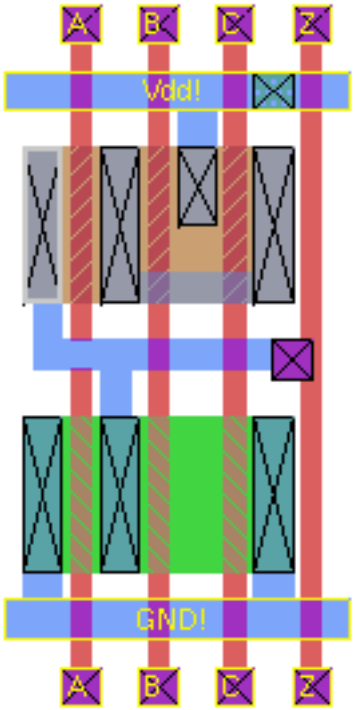
(B) Lower resistance.

(C) Better thermal expansion properties than metal.

(D) Makes a better contact to sources and drains.

(E) It simplifies the fabrication process.

Refer to the layout below for the next question (a color version of this layout is projected on the class-room's screen).



29. What is the logic function computed by this layout?

(A) NOT(C AND (B OR A))

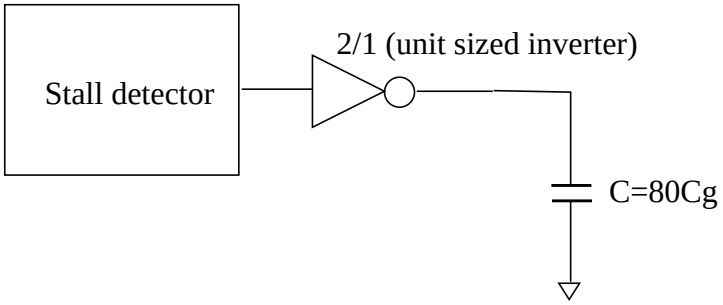
(B) NOT(C OR (B AND A))

(C) NOT(A AND (B OR C))

(D) NOT(A OR (B AND C))

(E) none of the above.

Next Question: You're designing the part of a microprocessor chip which transmits the "cache miss stall" signal to the other parts of the chip. The engineer who designed the circuit that detects the stall is gone SCUBA diving in Mexico, but left instructions that you're only permitted to load the output of the stall detector with a "unit sized inverter" which is an inverter with a PFET W/L=2/1 and NFET W/L=1/1. The situation that you face is drawn in the figure below. You've determined that the load of all of the other



chip modules which need to know about stall is equivalent to a capacitor with capacitance of 80 Cg, where Cg is the capacitance of a 1/1 sized gate. In other words, driving this load directly the unit sized inverter would see a load equal to about 27 unit-sized inverters. SPICE reports that driving this load with the unit sized inverter takes 8 ns for both the rising and falling edges. Unfortunately, this is many times longer than the cycle time of the processor. It's up to you to speed it up.

31. Given the information above, what is a good estimate for the delay of one unit sized inverter driving another unit sized inverter?

    (A) 3 ps

    (B) 30 ps

    (C) 300 ps

    (D) 3 ns

    (E) 30 ns

32. In practice, to speed this path you might make some adjustments to the stall circuit to beef up its ability to drive the load in question or use fancy signalling techniques to drive the large load. However, as a first cut, using only a chain of inverters (which likely will not all be unit sized), what is a good estimate of the minimum delay you could achieve driving the large load while still presenting the stall detector with a unit-sized inverter load?

    (A) 3 ps

    (B) 30 ps

    (C) 300 ps

    (D) 3 ns

    (E) 30 ns