Solid State Diodes

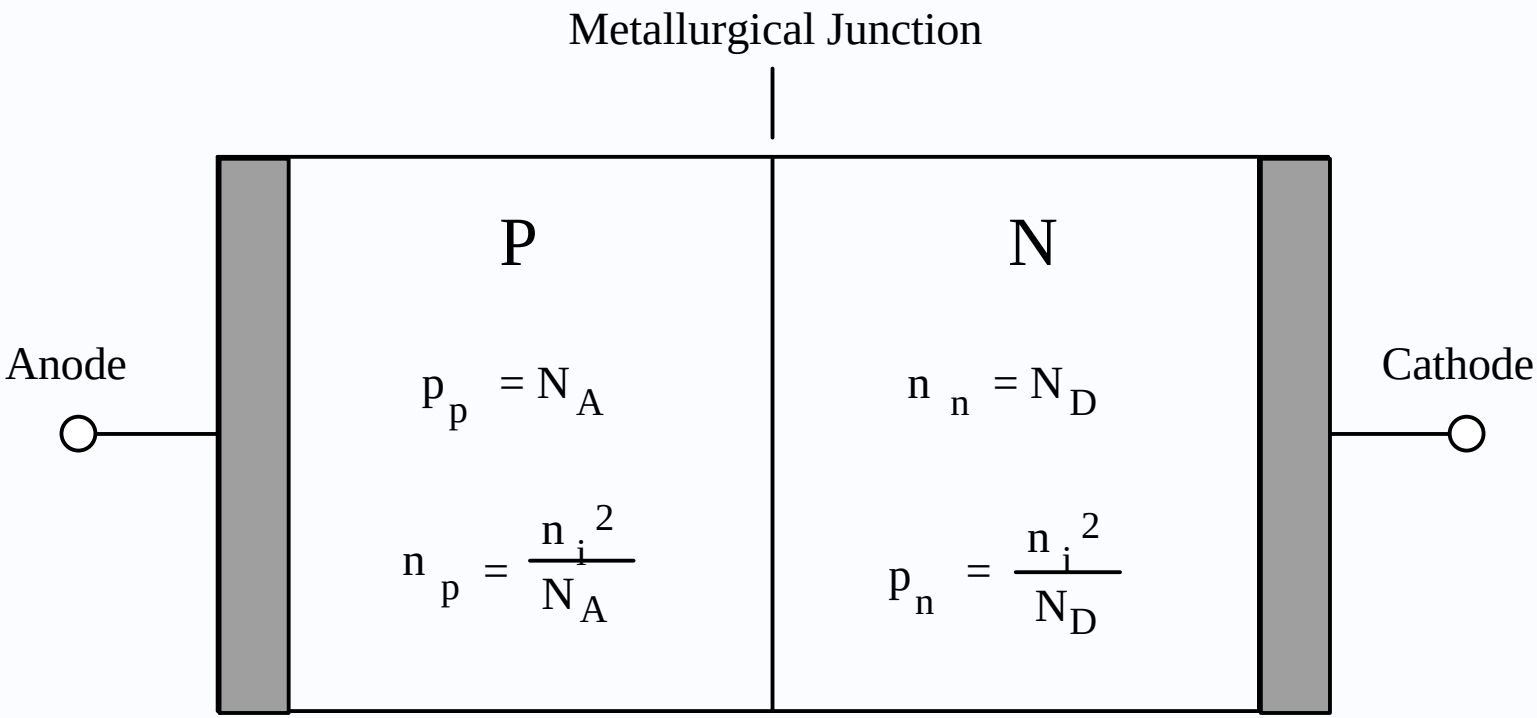


Figure 3.1 - Basic p-n junction diode

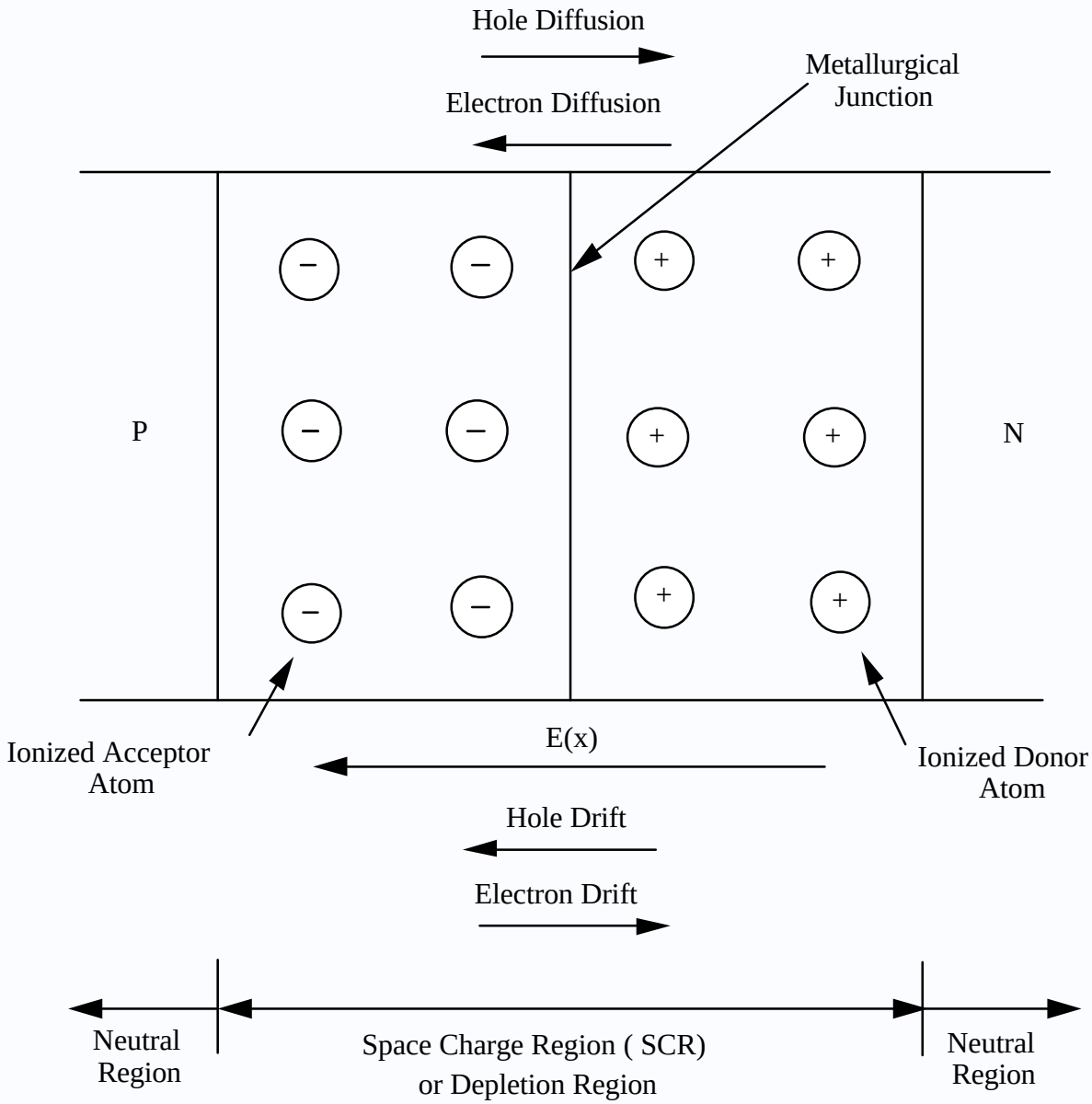


Figure 3.4 - Space charge region formation near the metallurgical junction

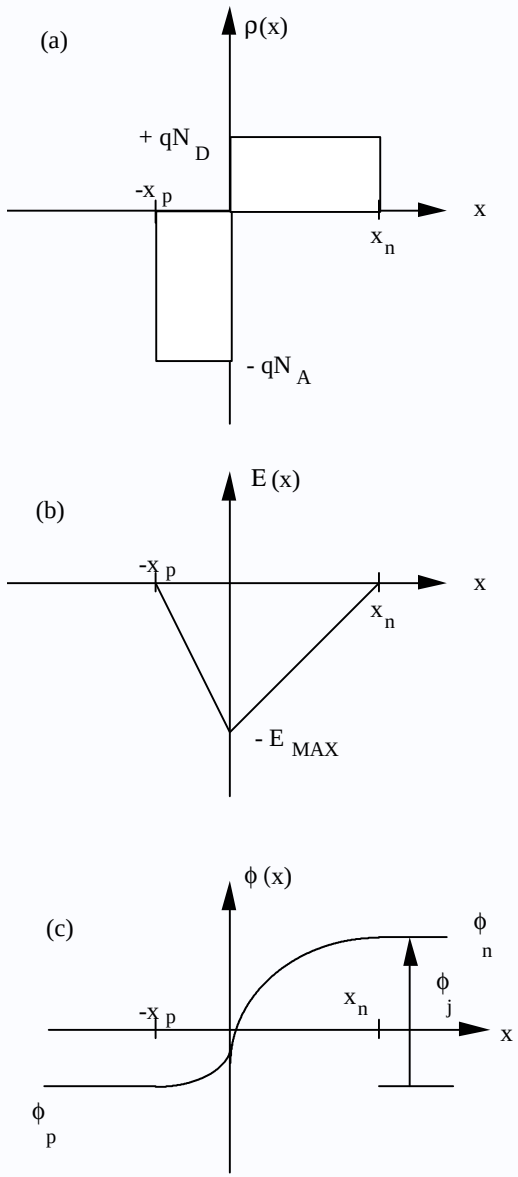


Figure 3.5 - (a) Charge density (C/ cm^3), (b) electric field (V/ cm) and (c) electrostatic potential (V) in the space charge region of p-n junction

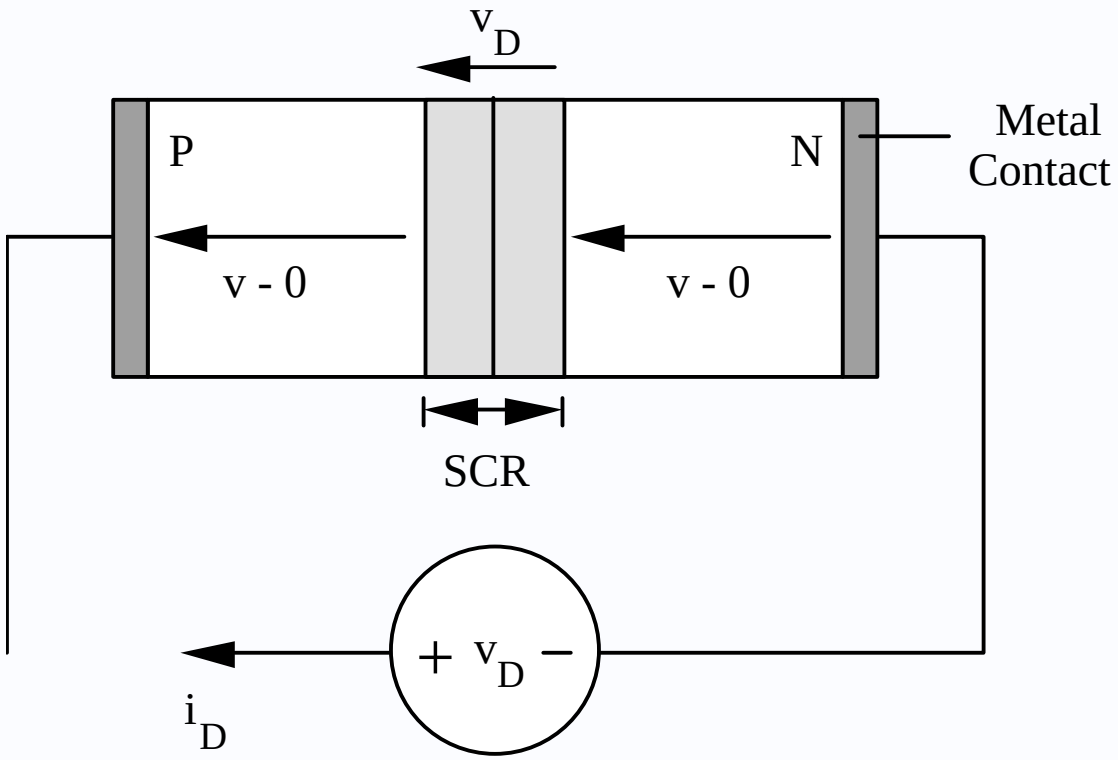


Figure 3.6 - Diode with external applied voltage v_D

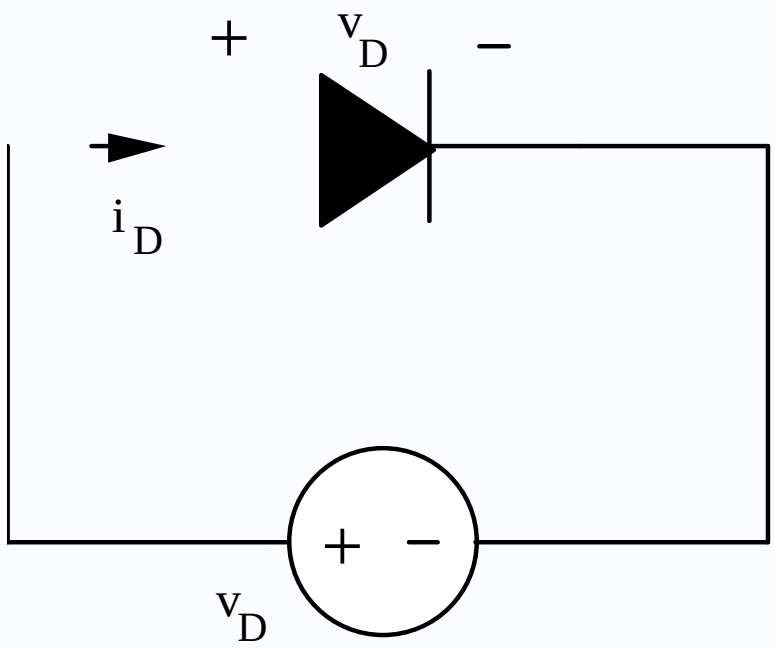


Figure 3.10 - Diode with applied voltage v_D

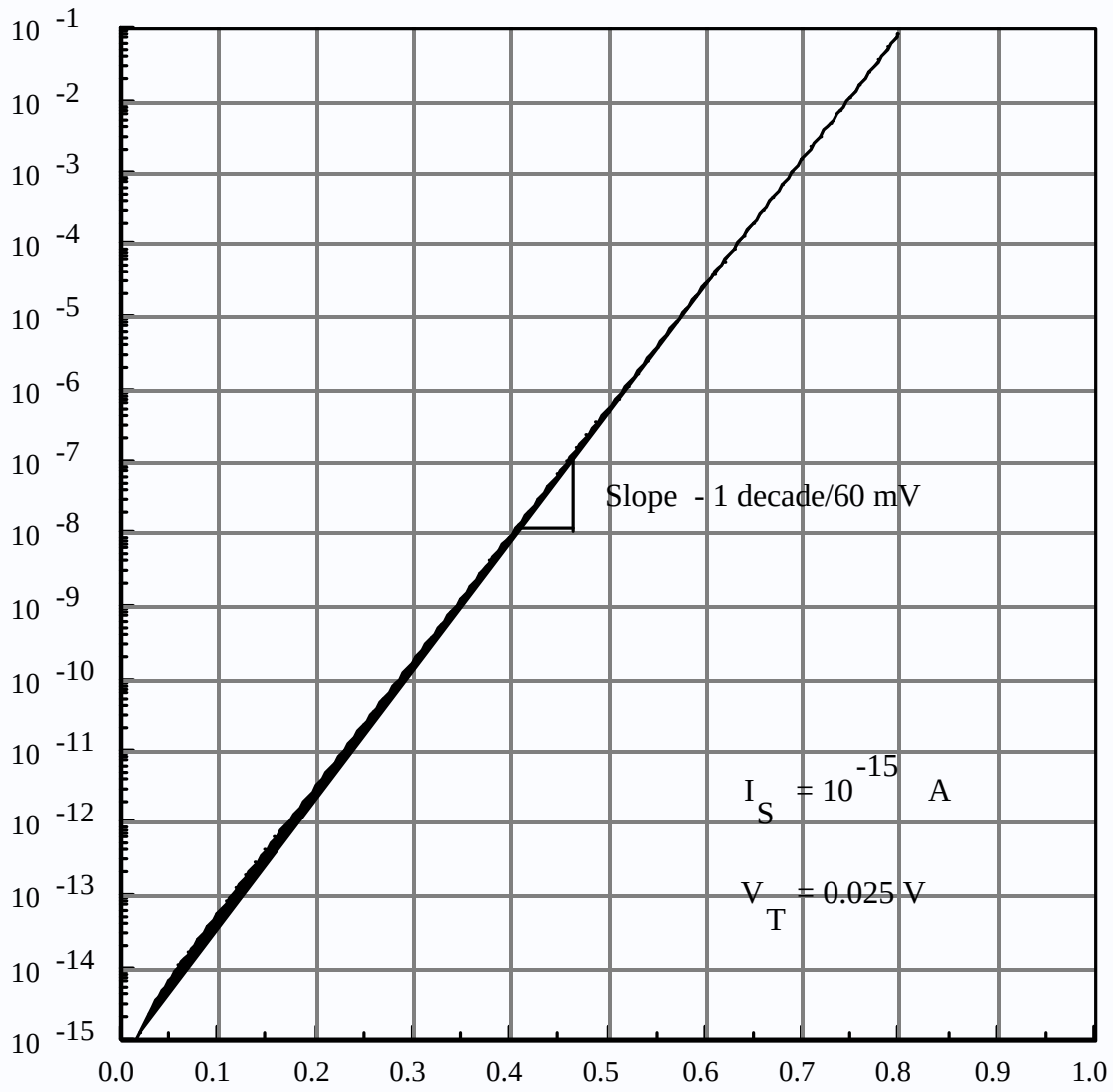


Figure 3.11 - Diode i-v characteristic on semilog scale

Diode Temperature Coefficient

- From the current equation

$$i_D = I_S \left[\exp\left(\frac{v_D}{V_T} \right) - 1 \right]$$

- we get for the diode in the forward bias

$$v_D = V_T \ln\left(\frac{i_D}{I_S} + 1 \right) = \frac{kT}{q} \ln\left(\frac{i_D}{I_S} + 1 \right) \approx \frac{kT}{q} \ln\left(\frac{i_D}{I_S} \right)$$

- so the temperature coefficient is

$$\frac{dv_D}{dT} = \frac{k}{q} \ln\left(\frac{i_D}{I_S} \right) - \frac{kT}{q} \frac{1}{I_S} \frac{dI_S}{dT} = \frac{v_D - V_{G0} - 3V_T}{T}$$

Diode Temperature Coefficient

- *where*

$$i_D >> I_S \approx n_i^2$$

and

$$V_{G0} = \frac{E_G}{q} \quad \textit{represents silicon bandgap energy at } 0K$$

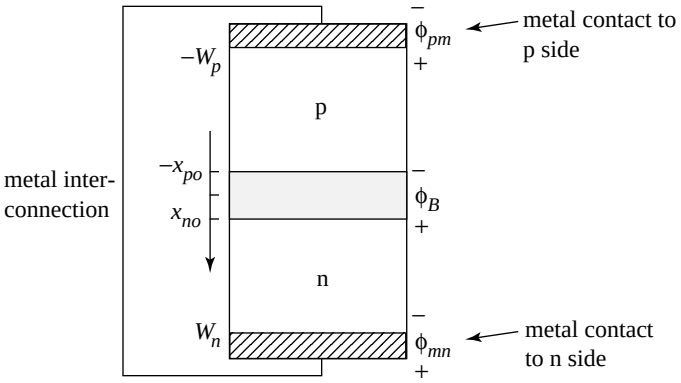
for silicon diode with $v_D = 0.65V$, $E_G = 1.12eV$,

and $V_T = 0.025V$

$$\frac{dv_D}{dT} = \frac{(0.65 - 1.12 - 0.075)V}{300K} = -1.82\ mV / K$$

pn Junction under Reverse Bias

- First, we must understand the *complete* structure of the pn junction-- starting in thermal equilibrium:



- How can $V_D = 0$ and the built-in potential barrier be $\phi_B = 1$ V (approx.)?

  Answer: look at the complete circuit ... including the potential barriers at the p-type silicon-to-metal (ϕ_{pm}) and the metal-to-n-type silicon (ϕ_{mn}) junctions.

- Kirchhoff's Voltage Law:

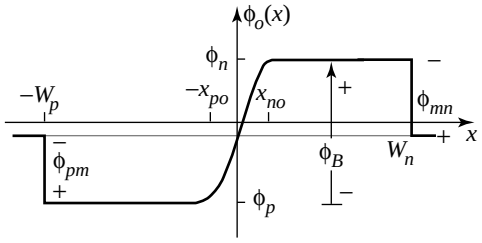
$$0 = \phi_{pm} + \phi_B + \phi_{mn}$$

  therefore, the built-in voltage is given by:

$$\phi_B = -\phi_{pm} - \phi_{mn}$$

Potential Plot through pn Junction

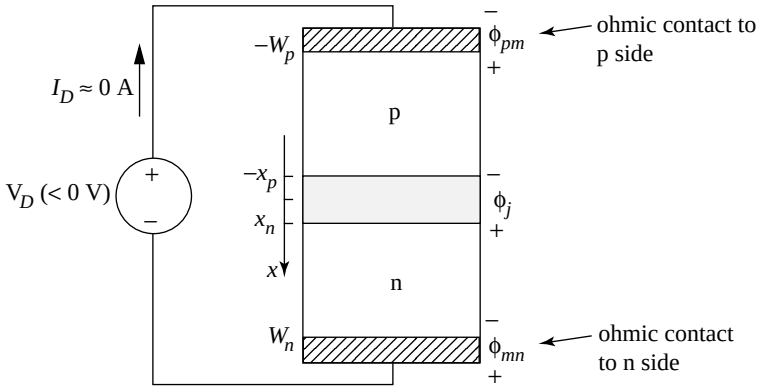
- The potential in the metal is the same on both ends of the pn junction in thermal equilibrium, with the metal-semiconductor contact potentials ("batteries") cancelling out the built-in potential



(b)

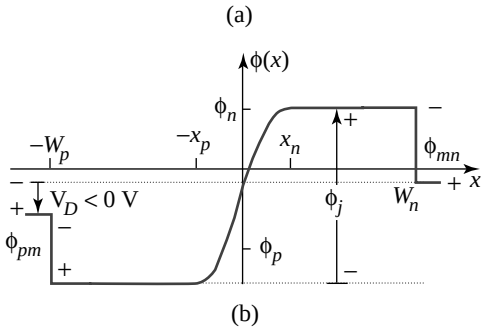
Note: we show potential changes at metal-silicon contacts as vertical, which is *not* correct. The details are left for an advanced device physics course.

- Now we apply a battery V_D ... with $V_D < 0$ (reverse bias)



pn Junction under Reverse Bias (cont.)

- Potential plot under reverse bias: contact potentials don't change ... they are *ohmic* contacts. Only place for change is at the pn junction

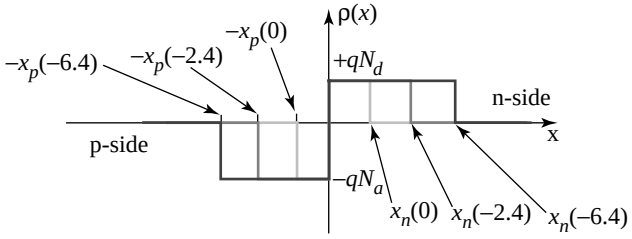


- The new potential barrier is called ϕ_j

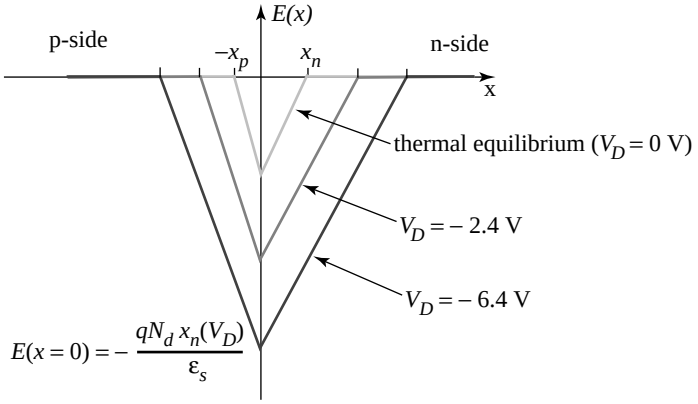
$$\text{KVL:} \qquad -V_D - \phi_{pm} - \phi_j - \phi_{mn} = 0$$

$$\phi_j = (-\phi_{pm} - \phi_{mn}) - V_D = \phi_B - V_D$$

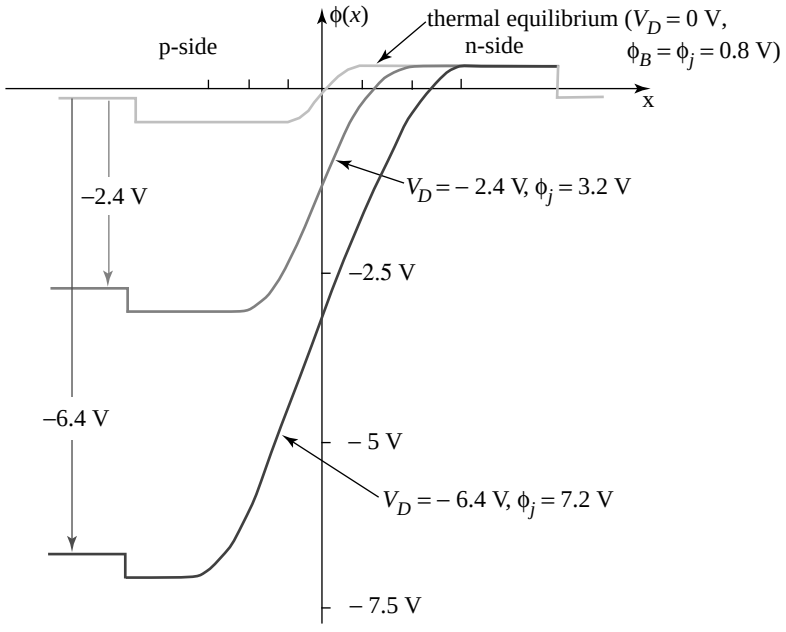
- The potential barrier is *increased* over the built-in barrier by the reverse bias ... which widens the depletion region ($x_n > x_{no}$, $x_p > x_{po}$)


ρ(x)
$-x_p(-6.4)$
$-x_p(-2.4)$
$-x_p(0)$
$+qN_d$
n-side
x
p-side
$-qN_a$
$x_n(0)$
$x_n(-2.4)$
$x_n(-6.4)$

(a)


E(x)
p-side
$-x_p$
x_n
n-side
x
thermal equilibrium ($V_D = 0$ V)
$V_D = -2.4$ V
$V_D = -6.4$ V
$E(x=0) = -\frac{qN_d\, x_n(V_D)}{\varepsilon_s}$

(b)


ϕ(x)
thermal equilibrium ($V_D = 0$ V,
$\phi_B = \phi_j = 0.8$ V)
p-side
n-side
x
$V_D = -2.4$ V, $\phi_j = 3.2$ V
–2.4 V
–2.5 V
–6.4 V
– 5 V
$V_D = -6.4$ V, $\phi_j = 7.2$ V
– 7.5 V

(c)

Quantitative Results

- Substitute ϕ_j for ϕ_B in the equilibrium depletion width and we find the depletion width under reverse bias (the math is the same):

$$x_p(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)} = x_{po}\sqrt{1 - (V_D/\phi_B)}$$

$$x_n(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{qN_d}\right)\left(\frac{N_a}{N_d + N_a}\right)} = x_{no}\sqrt{1 - (V_D/\phi_B)}$$

$$X_d(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = X_{do}\sqrt{1 - (V_D/\phi_B)}$$

- Note x_{po}, x_{no}, and X_{do} are the widths in thermal equilibrium

Avalanche breakdown

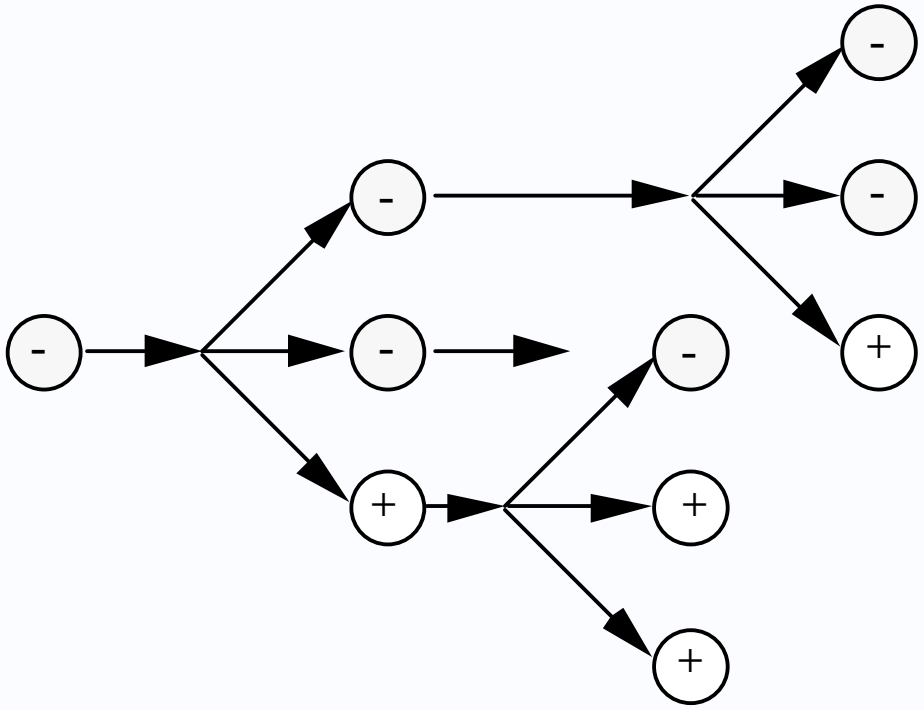


Figure 3.15 - The avalanche breakdown process. (Note that the positive and negative charge carriers will actually be moving in opposite directions in the electric field in the depletion region.)

Zener breakdown diode model

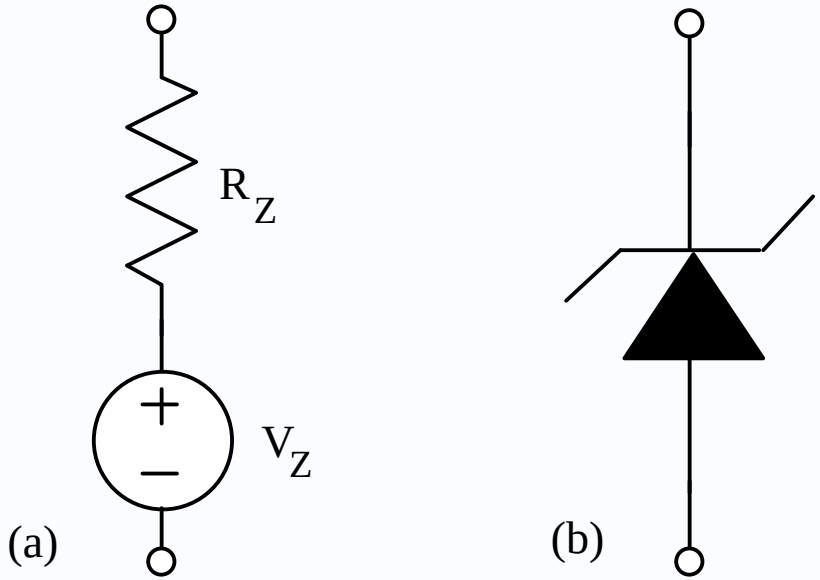


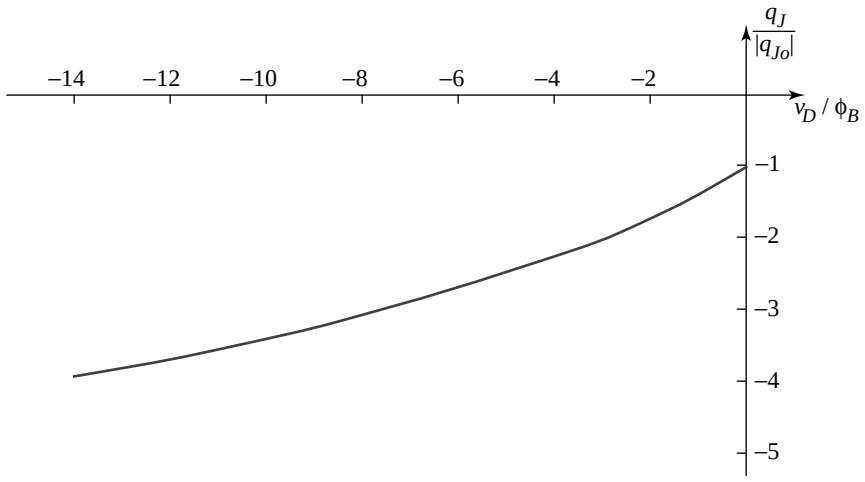
Figure 3.16 - (a) Model for reverse breakdown region of diode
(b) Zener diode symbol

Depletion Capacitance

- Find the function $q_J = q_J(v_D)$ from $x_p(v_D)$:

$$q_J(v_D) = -qN_a x_p(v_D) = -qN_a x_{po}\sqrt{1-(v_D/\phi_B)}$$

- Normalized plot:



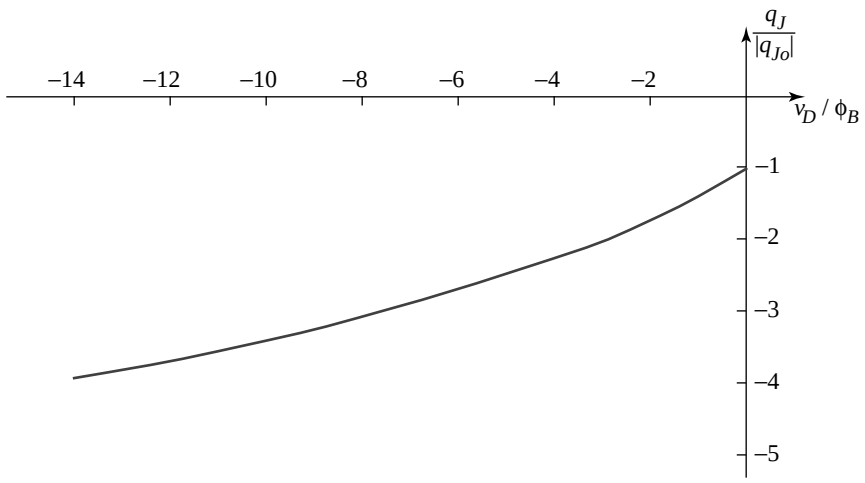
- To find the depletion capacitance C_j we simply take the derivative and evaluate it at the particular DC voltage

$$C_j = C_j(V_D) = \left.\frac{dq_J}{dv_D}\right|_{V_D}$$

- Math --> no insight into the *concept* of capacitance!

Graphical Interpretation

- Derivative is the *slope* of the plot of $q_J(v_D)$:

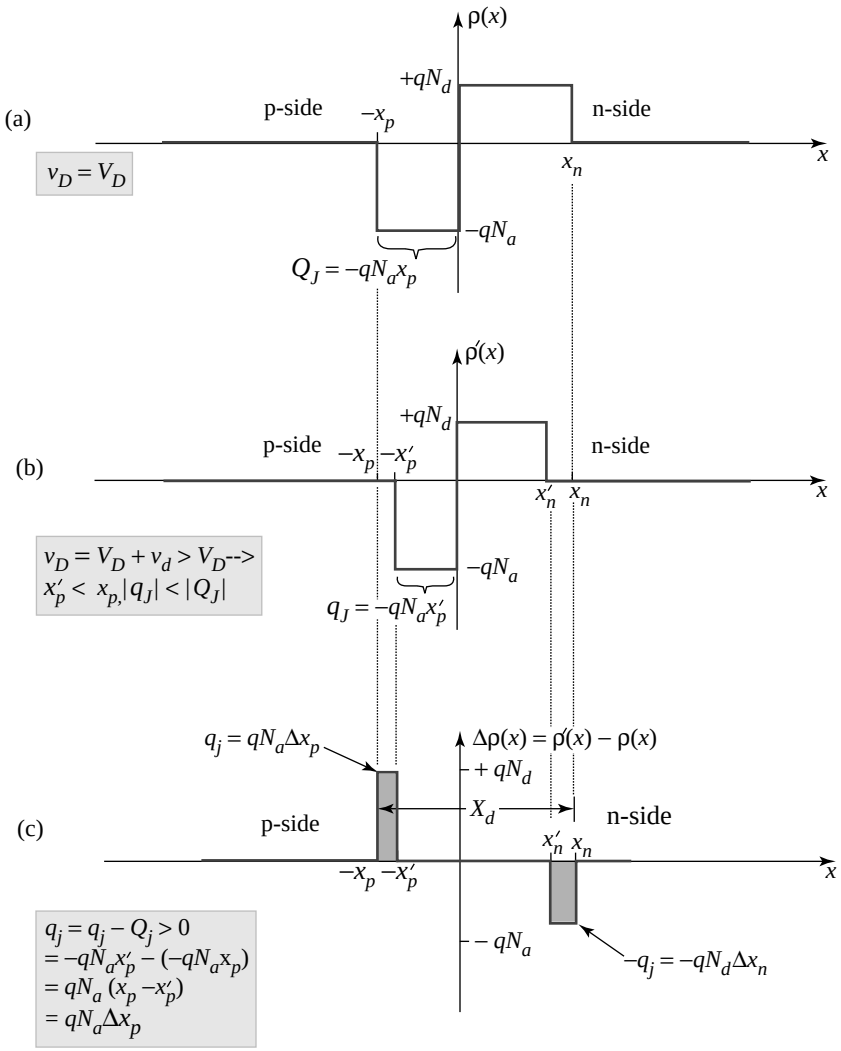


- The small-signal charge is related to the small-signal voltage by the slope at point (Q_J, V_J):

$$q_j = \left(\left. \frac{dq_J}{dv_D} \right|_{V_D} \right) \cdot v_d = C_j(V_D) \cdot v_d$$

Physical Interpretation

- Small-signal voltage changes the depletion width ($v_d > 0$ --> reverse bias is reduced --> depletion width is slightly narrower)

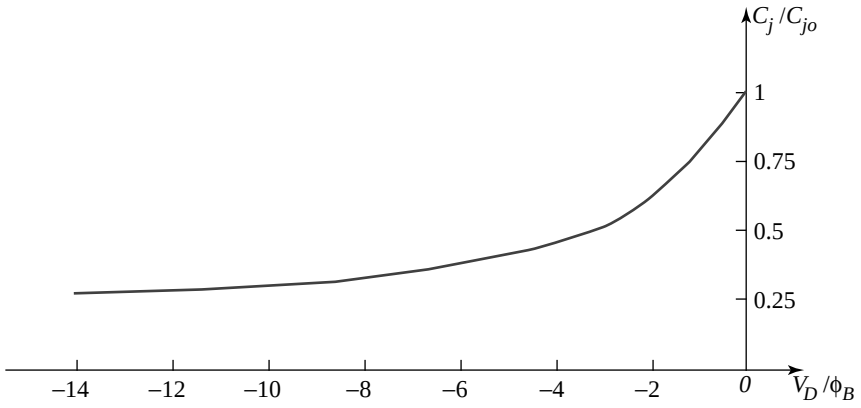


Depletion Capacitance Equation

- Derivative can be evaluated (see Chapter 3), but the incremental charge is two sheets separated by a distance $X_d(V_D)$ --> use parallel plate capacitor formula:

$$C_j = \frac{q_j}{v_d} = \frac{\varepsilon_s}{X_d(V_D)} = \frac{\varepsilon_s}{X_{do}\sqrt{1 - V_D/\phi_B}} = \frac{C_{jo}}{\sqrt{1 - V_D/\phi_B}}$$

- Plot of depletion capacitance (normalized to C_{jo}):



Typical numbers: X_{do} = 0.4 μm --> C_{jo} = 2.6 x 10^{-8} F/cm^2 = 0.26 fF/μm^2

ϕ_B = 0.8 V --> V_D = - 6.4 V = - 8 ϕ_B -->

$(1 - V_D / \phi_B)^{1/2}$ = 3 --> $C_j = C_{jo} / 3$ = 86 aF/μm^2

Variable capacitor diode

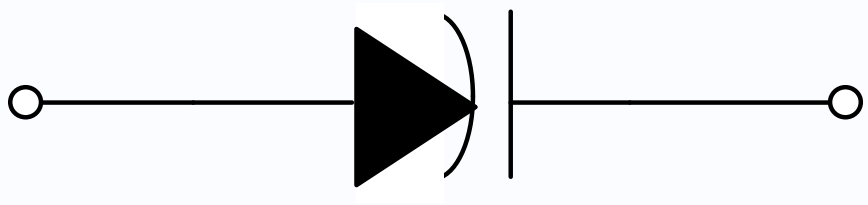


Figure 3.17 - Circuit symbol for the variable capacitance diode (varactor)

Schottky barrier diode

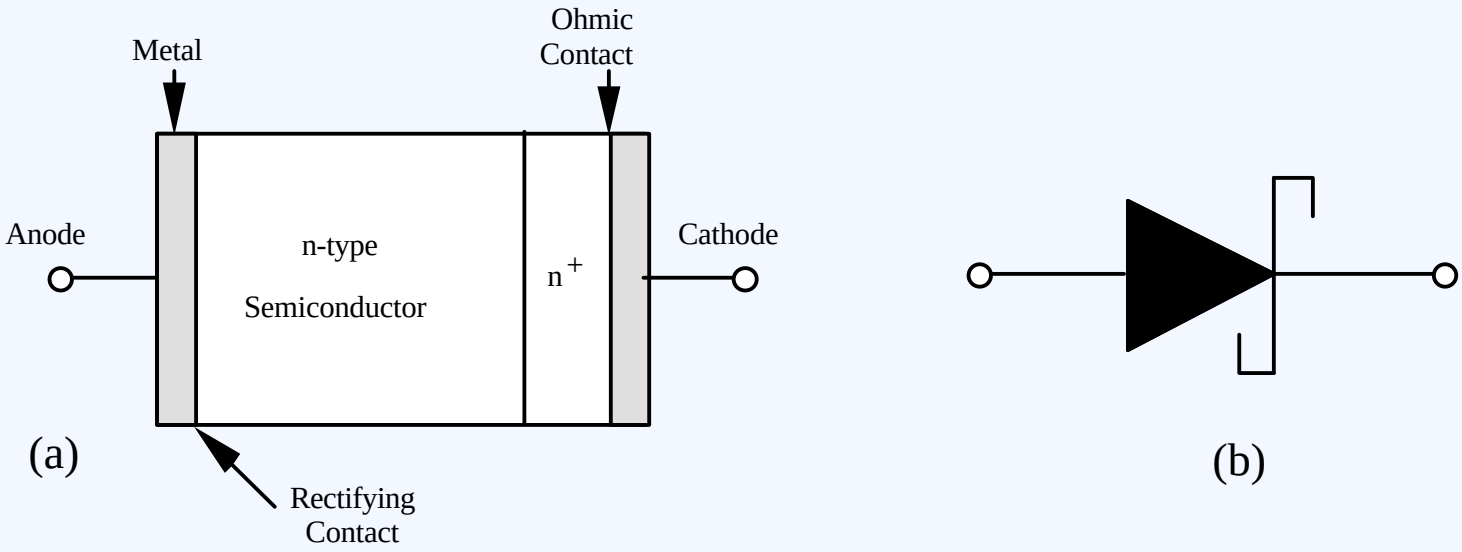


Figure 3.18 - (a) Schottky barrier diode structure
(b) Schottky diode symbol

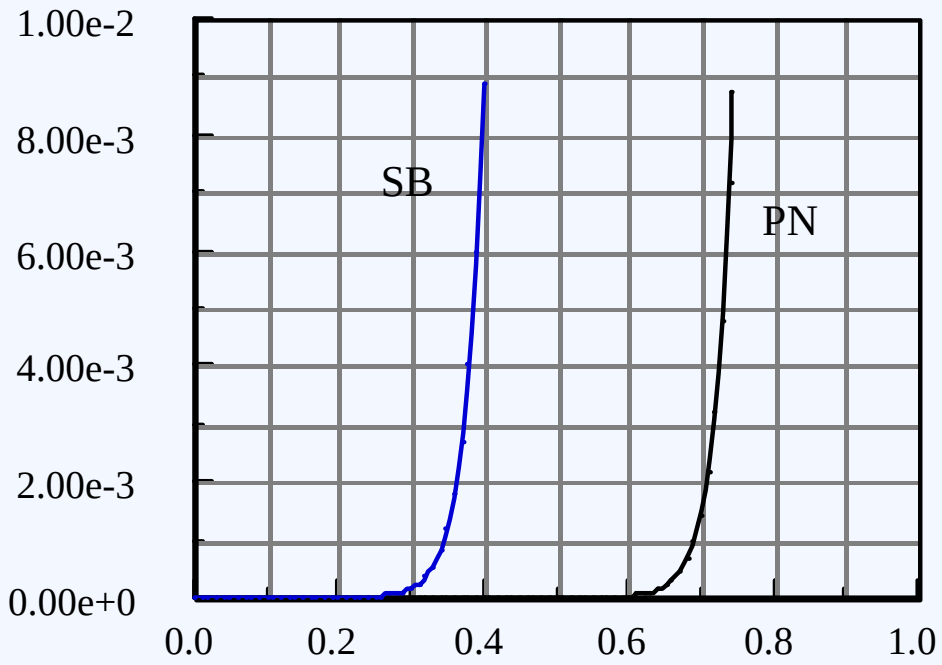


Figure 3.19 - Comparison of pn junction (PN) and Schottky diode (SB) i-v characteristics