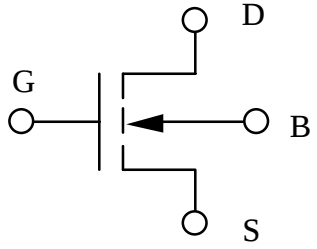
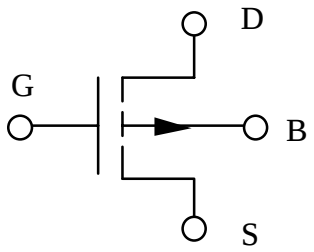
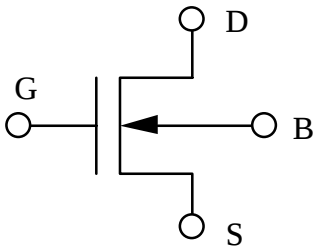
4.10 MOSFET circuit symbols and model summary



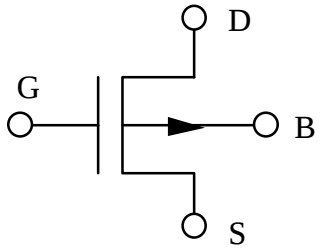
(a) NMOS enhancement-mode device



(b) PMOS enhancement-mode device

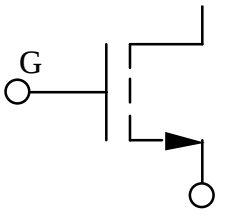


(c) NMOS depletion-mode device

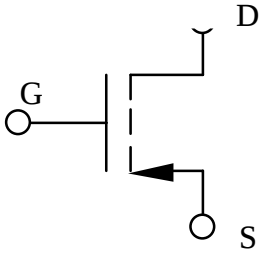


(d) PMOS depletion-mode device

Arrow points in the direction of



(e) Three-terminal NMOS transistor



(f) Three-terminal PMOS transistor

Arrow points in the direction of positive current

Figure 4.18 - IEEE Standard MOS transistor circuit symbols

Mathematical Model Summary

NMOS Transistor model summary

For all regions $K_n = \mu_n C_{ox}^{"} \frac{W}{L}$ $i_G = 0$ $i_B = 0$

Cutoff region:

$$i_{DS} = 0 \quad \textbf{for} \quad v_{GS} \le V_{TN}$$

Linear region:

$$i_{DS} = K_N (v_{GS} - V_{TN} - \frac{v_{DS}}{2}) v_{DS} \quad \textbf{for} \quad v_{GS} - V_{TN} \ge v_{DS} \ge 0$$

Saturation region:

$$i_{DS} = \frac{K_N}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS}) \quad \textbf{for} \quad v_{DS} \ge v_{GS} - V_{TN} \ge 0$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma (\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F})$$

PMOS transistor mathematical model summary

For all regions

$$K_n = \mu_n C''_{ox} \frac{W}{L} \qquad i_G = 0 \qquad i_B = 0$$

Cutoff region:

$$i_{SD} = 0 \quad \textbf{for} \quad v_{SG} \le -V_{TP} \; (v_{GS} \ge V_{TP})$$

Linear region:

$$i_{SD} = K_P (v_{SG} + V_{TP} - \frac{v_{SD}}{2}) v_{SD}$$

$$\textbf{for} \quad v_{SG} + V_{TP} \ge v_{SD} \ge 0$$

Saturation region:

$$i_{SD} = \frac{K_P}{2} (v_{SG} + V_{TP})^2 (1 + \lambda v_{SD}) \quad \textbf{for} \quad v_{SD} \ge v_{SG} + V_{TP} \ge 0$$

Threshold voltage:

$$V_{TP} = V_{TO} - \gamma (\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F})$$

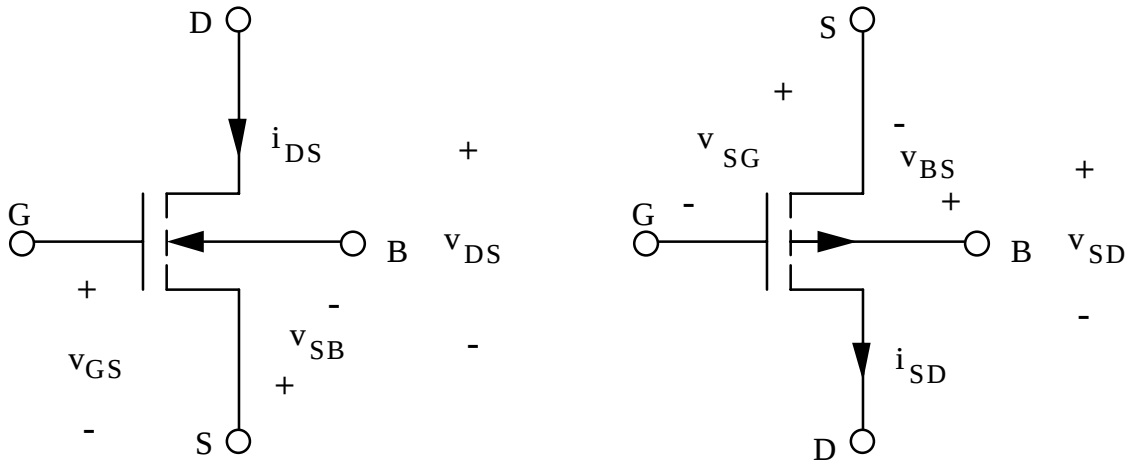


Figure 4.19 - NMOS and PMOS transistor circuit symbols

Table 4.1 - Categories of MOS Transistors

	NMOS Device	PMOS Device
Enhancement-mode	$V_{TN} > 0$	$V_{TP} < 0$
Depletion-mode	$V_{TN} <= 0$	$V_{TP} >= 0$

4.11 Biasing the MOSFET

An example biasing circuit

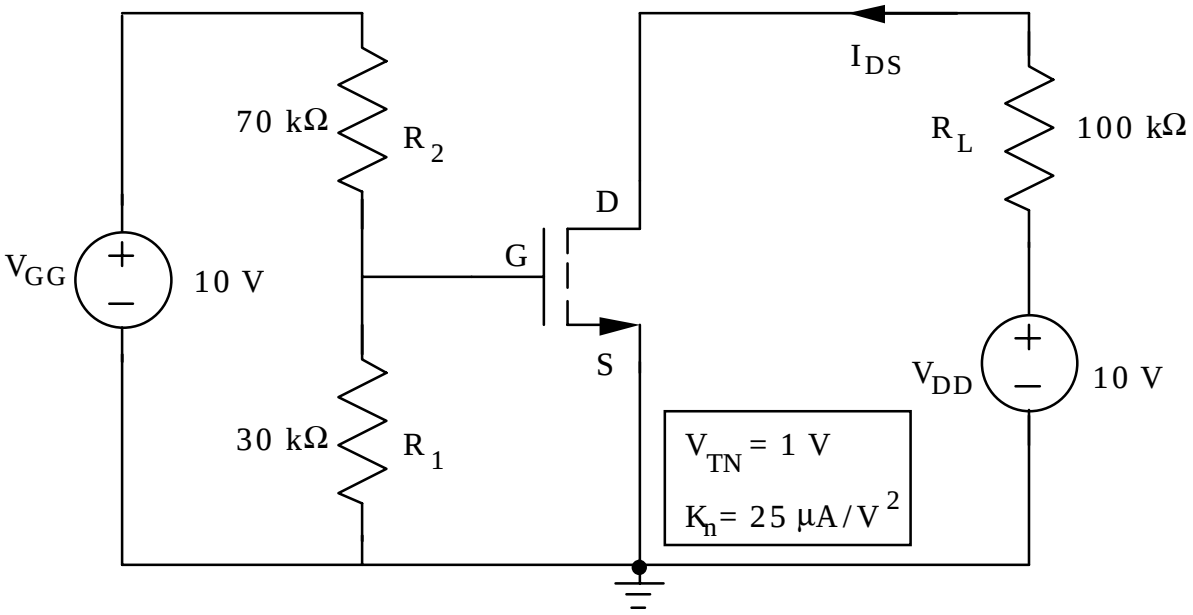


Figure 4.20 - Constant gate voltage bias using a voltage divider

Example 4.1

Find the Q-point using the mathematical model for the NMOS transistor

We replace the gate-bias network consisting of V_{GG}, R_1 and R_2 with its Thevenin equivalent circuit

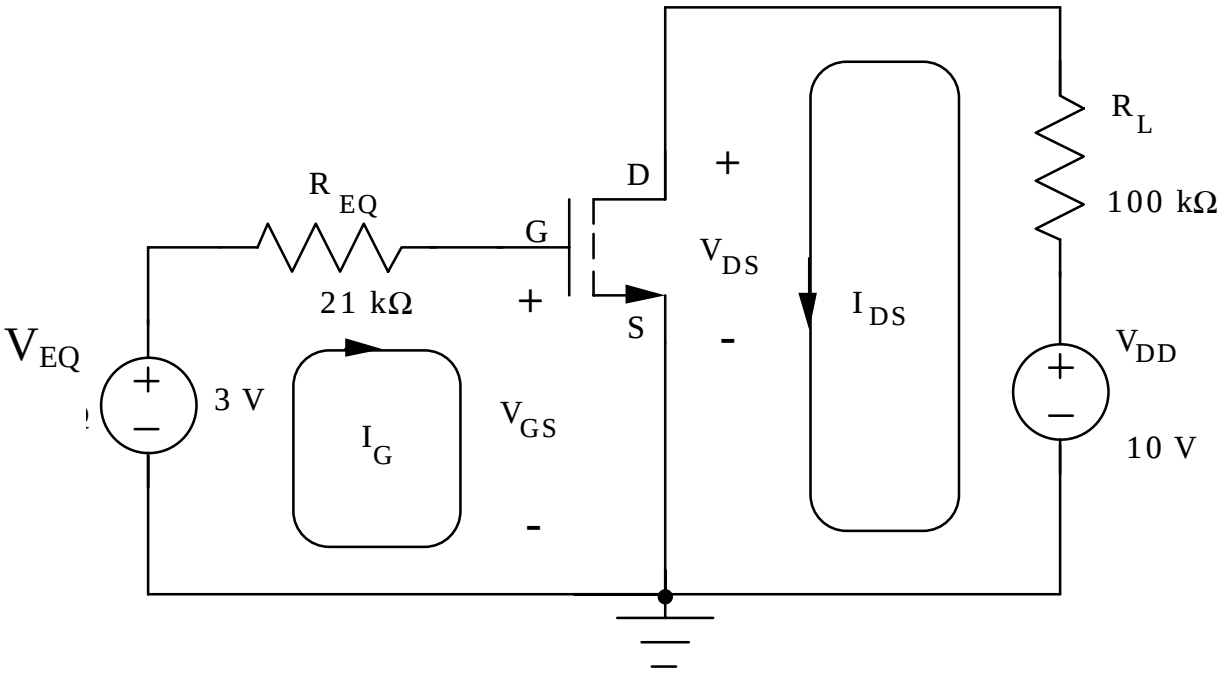


Figure 4.21 - Simplified MOSFET bias circuit

with

$$V_{EQ} = \frac{R_1}{R_1 + R_2} V_{GG} \quad \textbf{and} \quad R_{EQ} = \frac{R_1 R_2}{R_1 + R_2}$$

We can determine the Q-point by using Kirchhoff's voltage law (KVL) in the loops with V_{GS} and V_{DS}

$$V_{EQ} = I_G R_{EQ} + V_{GS} \quad \textbf{(*)}$$

$$V_{DD} = I_{DS} R_L + V_{DS}$$

We know for the MOSFET, however that $I_G = 0$ so that $V_{GS} = V_{EQ} = 3V$ and we get

$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2 = 50\ \mu A$$

and

$$V_{DS} = V_{DD} - I_{DS}R_L = 5V$$

$$V_{GS} - V_{TN} = 2V$$

We see that V_{DS} exceeds $V_{GS} - V_{TN}$ so that the transistor is indeed saturated. Thus, the Q-point is $(50\mu A, 5V)$, with $V_{GS} = 3V$.

Example 4.2

The Q-point for the MOSFET circuit in Fig.4.20 can also be found graphically with a load-line method. The second expression in Eq.(*) represents the load line for this MOSFET circuit:

$$V_{DD} = I_{DS}R_L + V_{DS}$$

or

$$10 = 10^5 I_{DS} + V_{DS}$$

The load-line is constructed by finding two points:

for $V_{DS} = 0, I_{DS} = 100\mu A$, and for $I_{DS} = 0, V_{DS} = 10V$. The resulting line is drawn on the output characteristics of the MOSFET in Fig.4.22

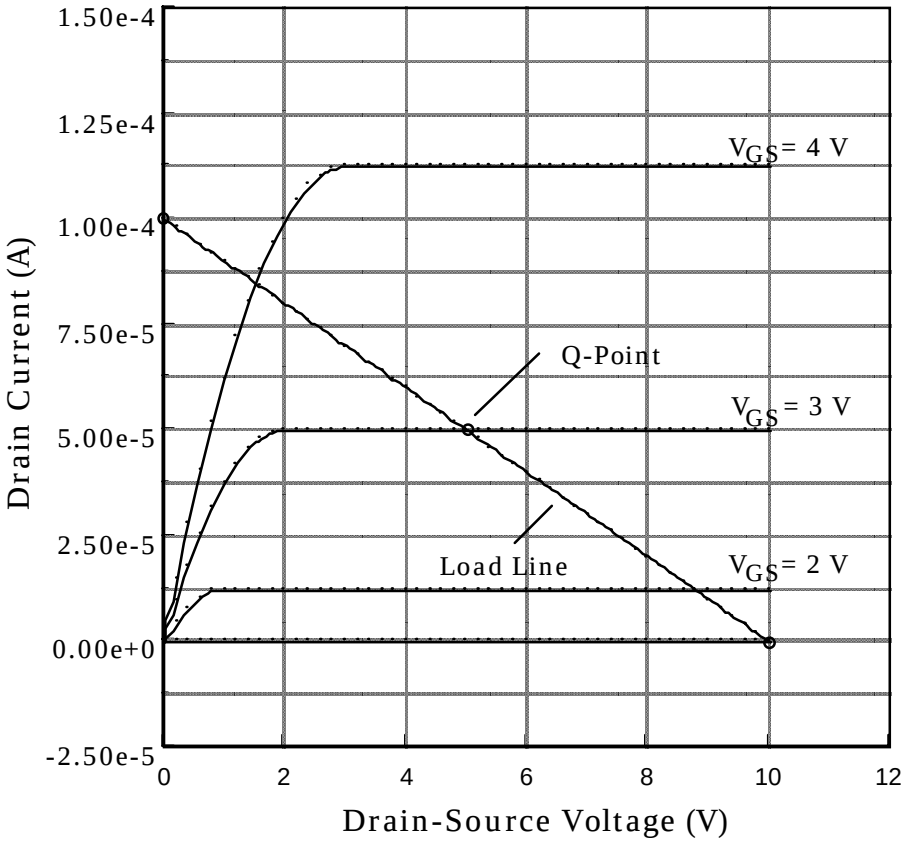


Figure 4.22 - Load line for the circuit in Figs. 4.20 and 4.21

Example 4.3

The I-v characteristic of an ideal current source is shown in Fig.4.23 which provides a constant output

current regardless of the polarity of the voltage across the source.

If the value of V_{DD} is chosen to be larger than the value needed to pinch off the MOSFET [in this case, $V_{DD} \geq (V_{GS} - V_{TN}) = 3 - 1 = 2V$], then the output current will be constant at 50 μA. For $V_{DD} \geq 2V$, the MOSFET represents an electronic current source with a 50 μA output current.

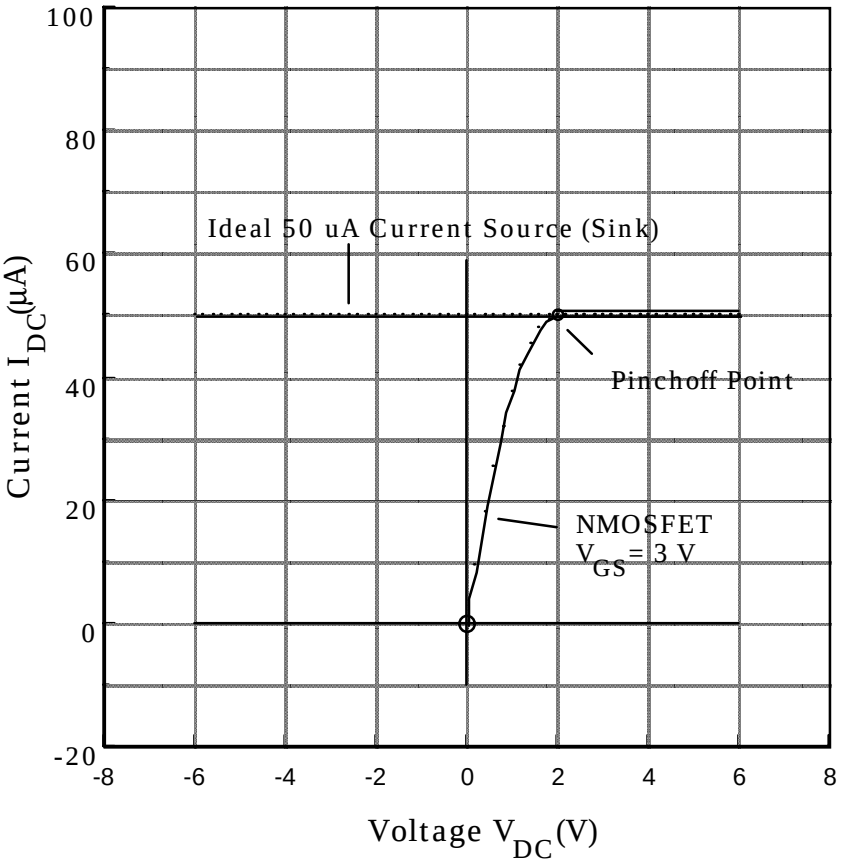


Figure 4.23 - Output characteristics for an ideal current source and the MOSFET current source

Figure 4.24 shows the NMOS transistor biased with a 3-V dc source. This simple two-terminal MOSFET circuit will behave as an electronic current source

$$I_{DC} = I_{DS} = 50\mu A$$

over a limited range of terminal voltage, as long as the external voltage V_{DC} exceeds 2V.

Here, the current enters the source and it is often referred to as a current sink.

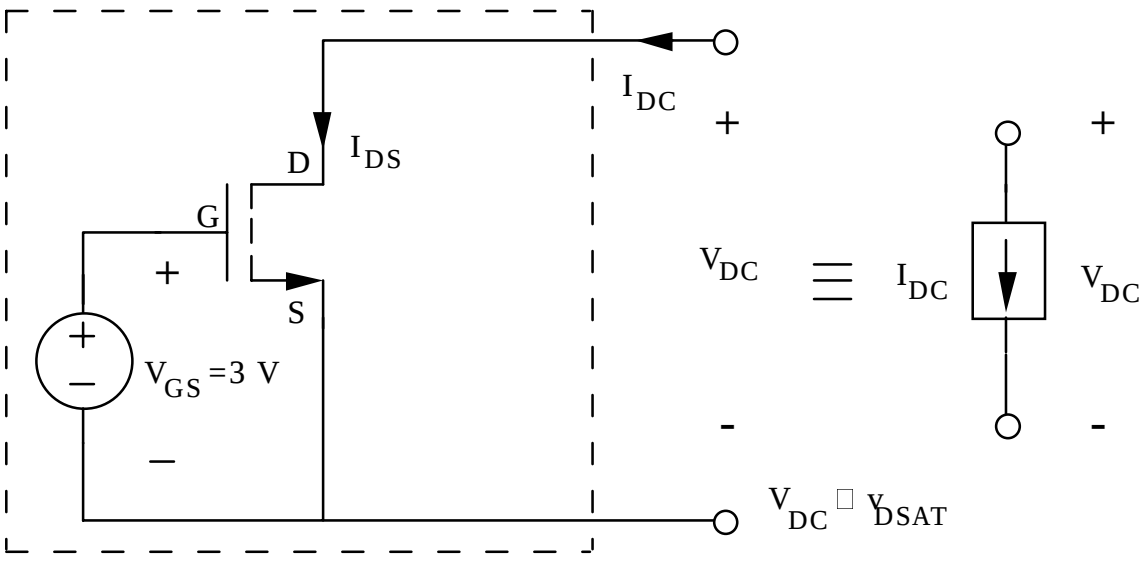


Figure 4.24 - NMOS transistor as an electronic current source

Example 4.4

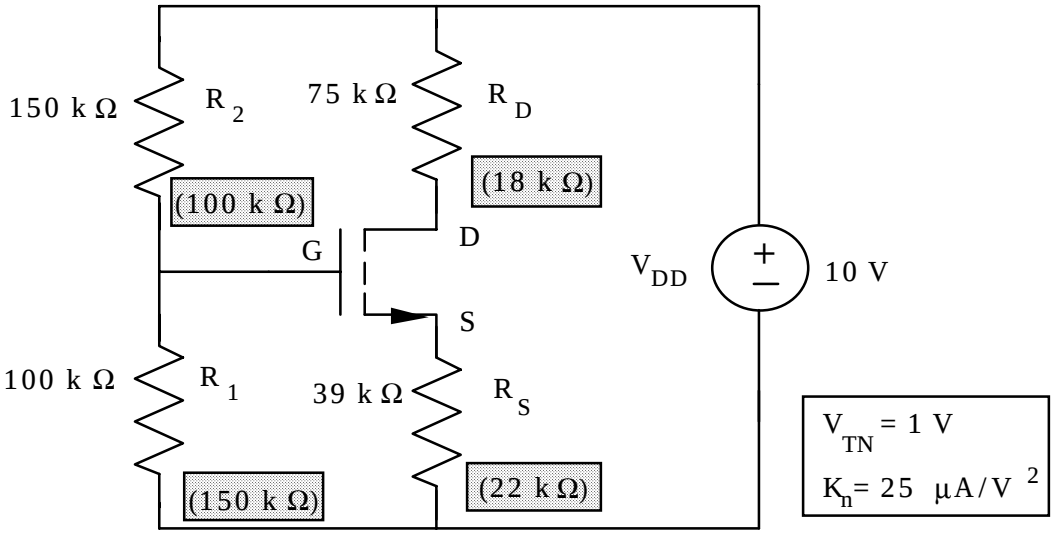


Figure 4.25(a) - Four resistor bias network for a MOSFET

The four-resistor bias circuit in Fig.4.25(a) will stabilize the MOSFET Q-point in the face of many types of circuit parameter variations. A single voltage source V_{DD} is now used to supply both the gate-bias voltage and drain current.

A Thevenin transformation is applied to this circuit, resulting in the equivalent circuit given in Fig.4.26. This is the final circuit to be analyzed.

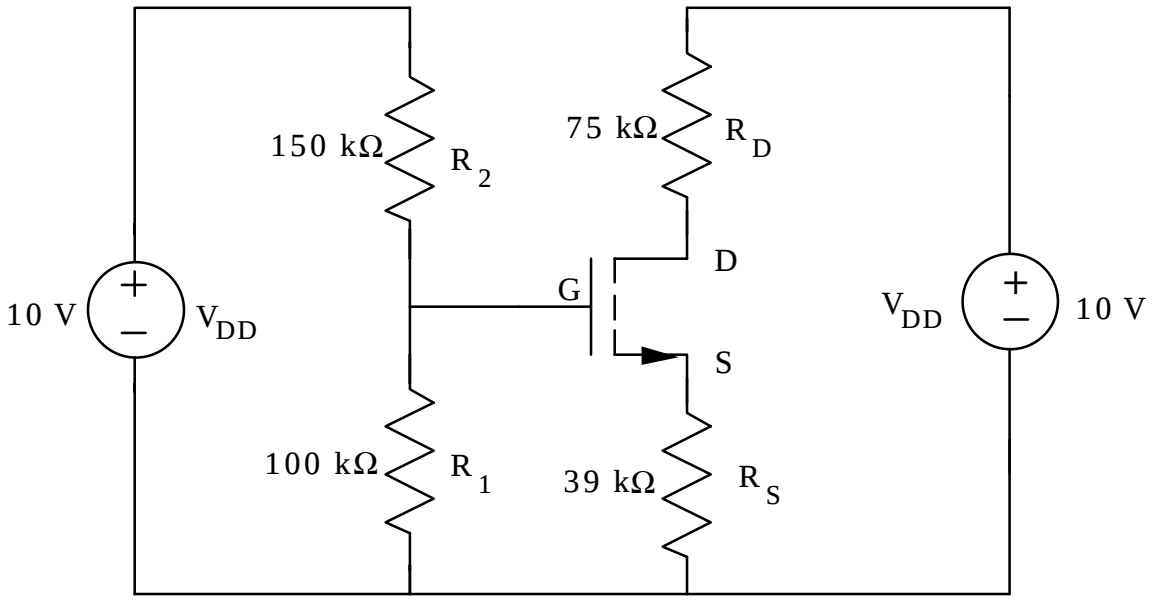


Figure 4.25(b) - Equivalent circuit with replicated sources

Note that this circuit uses the three-terminal representation for the MOSFET in which it is assumed that the bulk terminal is tied to the source. If the bulk terminal were grounded, the analysis would become more complex because the threshold voltage would then be a function of the voltage developed at the source terminal of the device.

To determine the Q-point for the circuit in Fig.4.26, we write the following two loop equations:

$$V_{EQ} = I_G R_{EQ} + V_{GS} + (I_G + I_{DS})R_S$$

$$V_{DD} = I_{DS} R_D + V_{DS} + (I_G + I_{DS})R_S$$

Because we know that $I_G = 0$ **,these equations reduce to**

$$V_{EQ} = V_{GS} + I_{DS} R_S$$

$$V_{DD} = I_{DS}(R_D + R_S) + V_{DS}$$

Again assuming that the transistor is operating in the saturation region with

$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2$$

the input loop equation becomes

$$V_{EQ} = V_{GS} + \frac{K_n R}{2}(V_{GS} - V_{TN})^2$$

and we have a quadratic equation to solve for V_{GS} **.For the values in Fig.4.25 with** $V_{TN} = 1V$ **and**

$$K_n = 25\mu A/V^2$$

So we get $V_{GS} = \pm 2.66V$ **For** $V_{GS} = -2.66V$ **,the MOSFET would be cut off because** $v_{GS} < V_{TN}$ **. So,** $V_{GS} = +2.66V$ **is the answer, and** $I_{DS} = 34.4\mu A$ **.** V_{DS} **is then found to be 6.08V. We have**

$$V_{DS} = 6.08V, \quad V_{GS} - V_{TN} = 1.66V \qquad V_{DS} \geq (V_{GS} - V_{TN})$$

The saturation region assumption is consistent with the resulting Q-point: $(34.4\mu A, 6.08V)$ **with** $V_{GS} = 2.66V$

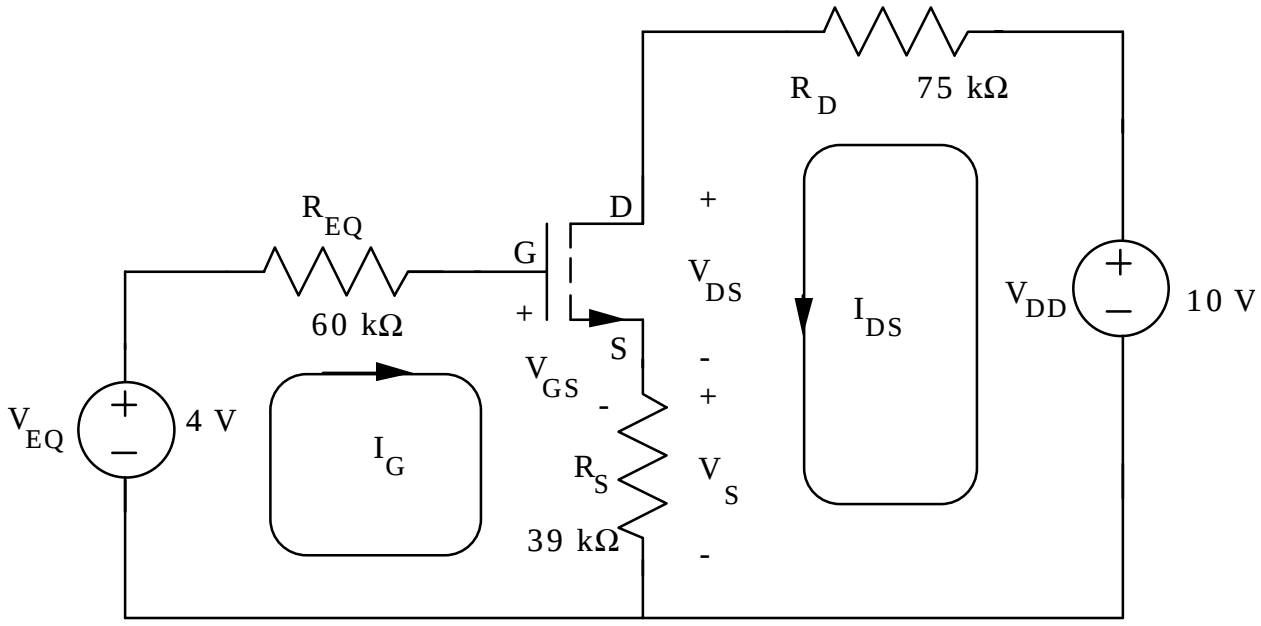


Figure 4.26 - Equivalent circuit for the four resistor bias network

Example 4.5

Let us redesign the four-resistor bias network in the previous example to increase the current while keeping V_{DS} approximately the same: the desired Q-point will be $(100\mu A, 6V)$. We can see that the sum of

R_D and R_S in the bias network of Fig.4.26 is determined by the Q-point values

$$R_D + R_S = \frac{V_{DD} - V_{DS}}{I_{DS}} = 40K\Omega$$

The required value of R_S

$$R_S = \frac{V_{EQ} - V_{GS}}{I_{GS}} = \frac{V_S}{I_{DS}}$$

But we must first find the value of V_{GS}

The gate-source voltage needed to establish $I_{DS} = 100\mu A$ can be found by rearranging the expression for the MOSFET drain current,

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_{DS}}{K_n}} = 3.83V$$

So Rs=1.7 $K\Omega$