Chapter 4

Field-Effect Transistors

Metal-oxide semiconductor field effect transistor (MOSFET)

and

Junction field-effect transistor (JFET)

4.1 Characteristics of the MOS capacitor

MOS capacitor is essential to MOS transistor operation

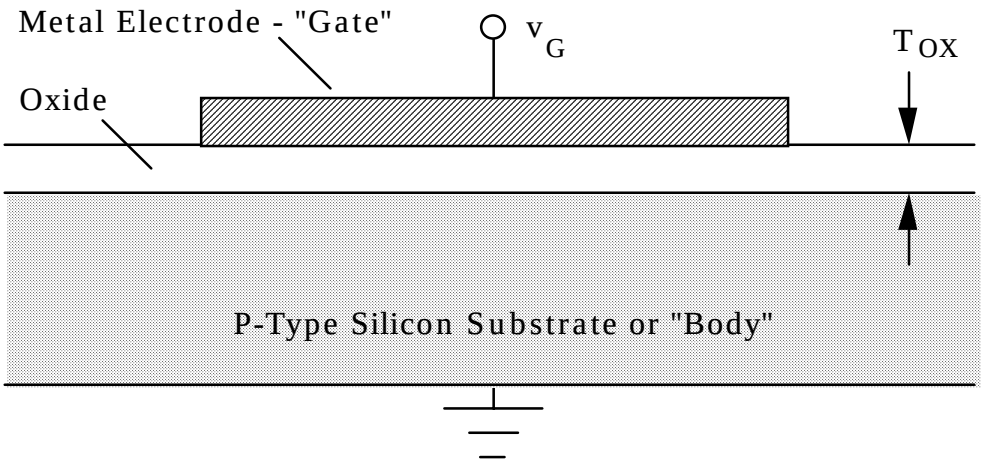
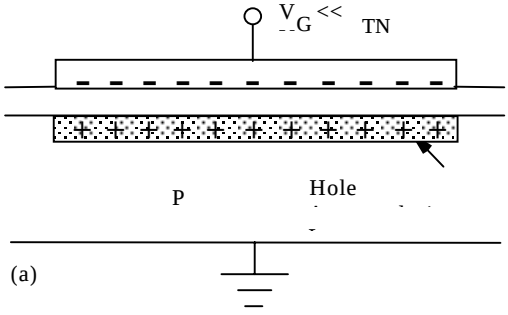
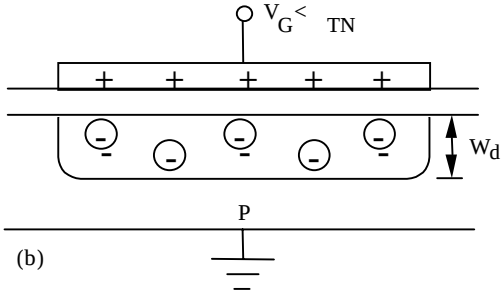


Figure 4.1 - MOS capacitor structure on p-type silicon

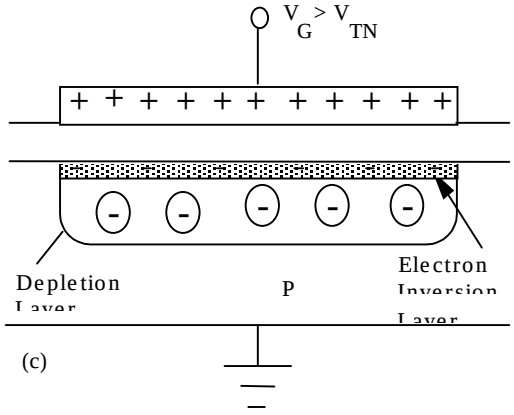
Accumulation Region



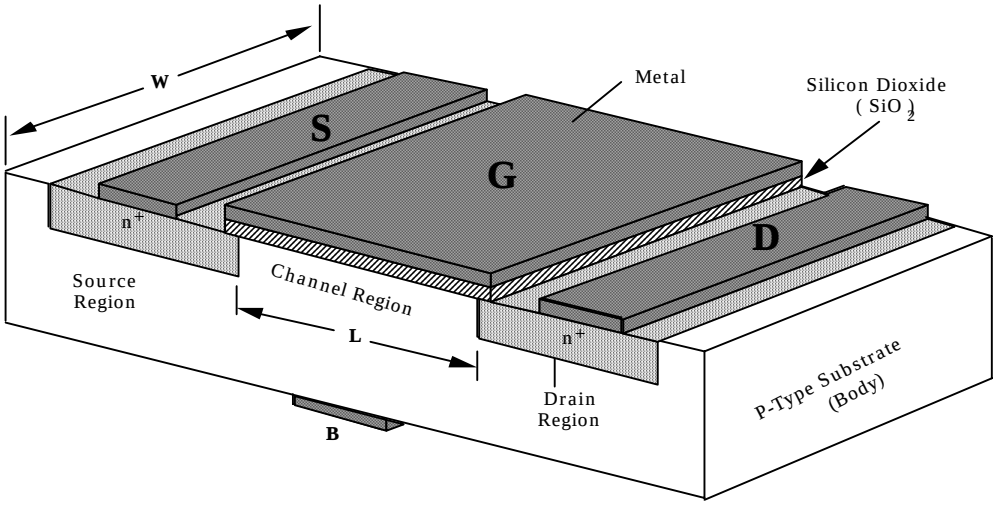
Depletion Region



Inversion Region



4.2 Structure of the NMOS transistor



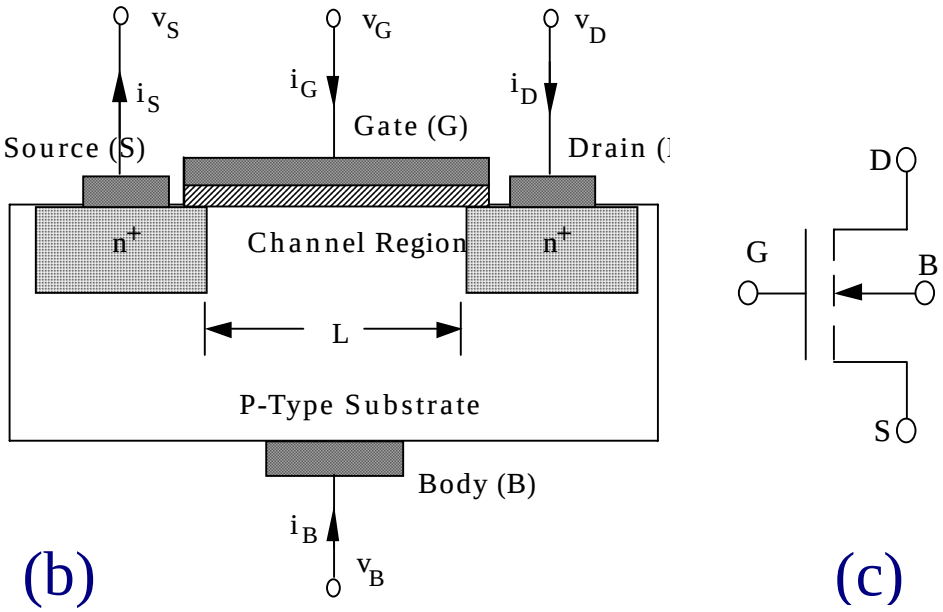


Figure 4.3 - (a) NMOS transistor structure (b) cross section and (c) circuit symbol

4.3 Qualitative *I-v* behavior of the NMOS transistor

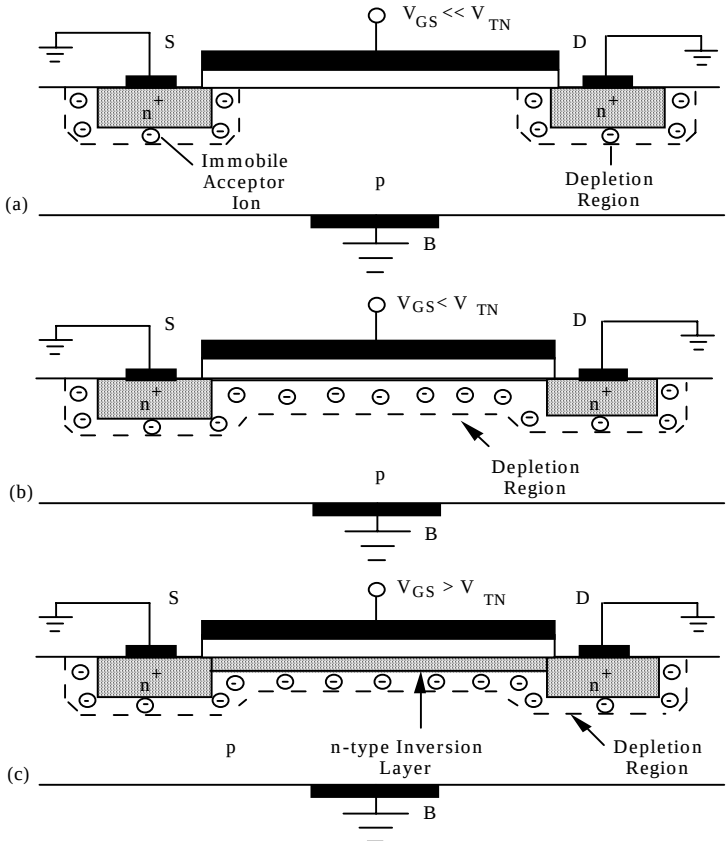


Figure 4.4 - (a) $V_{GS} << V_{TN}$ (b) $V_{GS} < V_{TN}$ (c) $V_{GS} > V_{TN}$

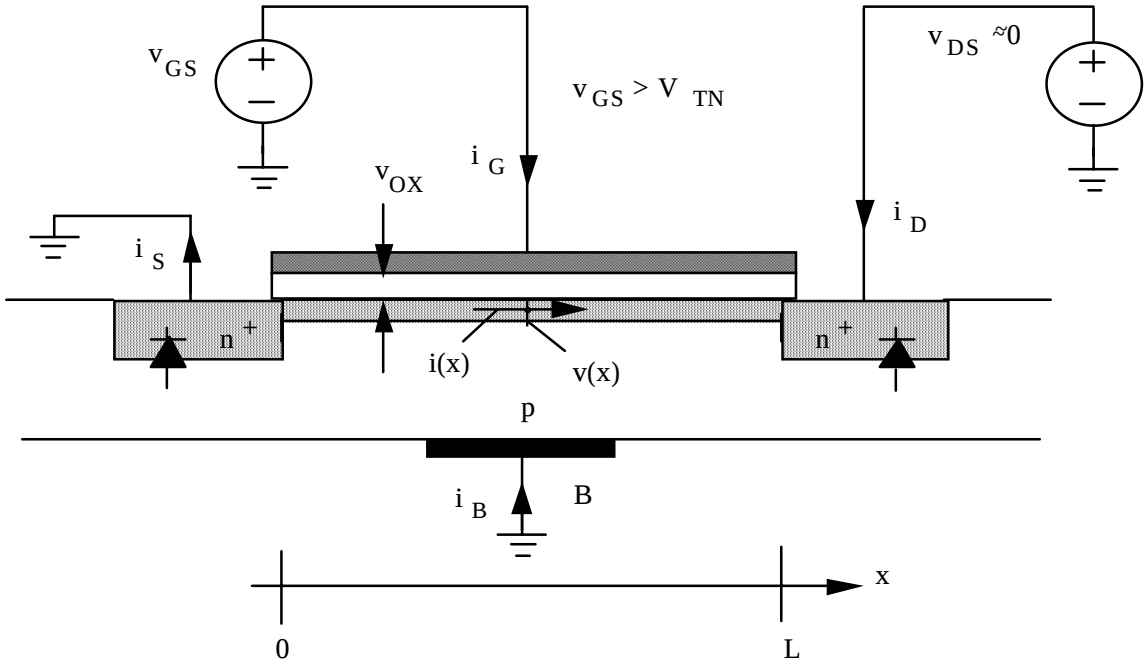


Figure 4.5 - Model for determining i-v characteristics of the NMOS transistor

4.4 Linear region characteristics of the NMOS transistor

The electron charge per unit length at point x

$$Q' = -WC''_{OX}(v_{ox} - V_{TN}) \quad C/cm \quad \textbf{for} \quad v_{ox} >= V_{TN} \qquad \textbf{(*)}$$

where $C''_{OX} = \varepsilon_{OX} / T_{OX}$ **, oxide capacitance per unit area** ($\mathrm{F/cm^2}$)

ε_{OX} = **oxide permittivity** $(F/cm)^1$

T_{OX} = **oxide thickness** *(cm).*

v_{ox} **represents the voltage across the oxide and is a function of position** x **in the channel**

$$v_{OX} = v_{GS} - v(x)$$

where

$v(x)$ **= voltage at any point** x **in the channel referred to the source**

Note that v_{ox} **must exceed** V_{TN} **for an inversion layer to exist, so** Q' **will be zero until** $v_{ox} > V_{TN}$ **.**

At the source end of the channel $v_{OX} = v_{GS}$ **, and it decreases to** $v_{OS} = v_{GS} - v_{DS}$ **at the drain end of the channel.**

The electron drift current at any point in the channel is given by the product of the charge per unit length times the velocity v_x

$$i(x) = Q'(x)v_x(x)$$

The charge Q' **is represented by Eq.(*) and the velocity** v_x **of electrons in the channel is determined**

by the electron mobility and the transverse electric field in the channel, so

$$i(x) = Q'v_x = [-WC''_{OX}(v_{OX} - V_{TN})][-\mu_n E_x]$$

The transverse electric field is equal to the negative of the spatial derivative of the voltage in the channel

$$E_x = -\frac{dv(x)}{dx}$$

So the current at any point in the channel

$$i(x) = -\mu_n C''_{OX} W(v_{GS} - v(x) - V_{TN})]\frac{dv(x)}{dx}$$

$$i(x)dx = -\mu_n C''_{OX} W(v_{GS} - v(x) - V_{TN})]dv(x)$$

Integrating $i(x)$ **along the channel, we get**

$$i_{DS} = \mu_n C''_{OX} \frac{W}{L}(v_{GS} - V_{TN} - \frac{v_{DS}}{2})v_{DS}$$

or

$$i_{DS} = K'_N \frac{W}{L}(v_{GS} - V_{TN} - \frac{v_{DS}}{2})v_{DS}$$

where $K'_n = \mu_n C''_{ox}$ **and** $V_{GS} - V_{TN} >= V_{DS} >= 0$

or

$$i_{DS} = K_N\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \quad \textbf{where} \quad K_n = K_n^{'}\frac{W}{L}$$

Interpretation of the Linear Region *I-V* characteristic

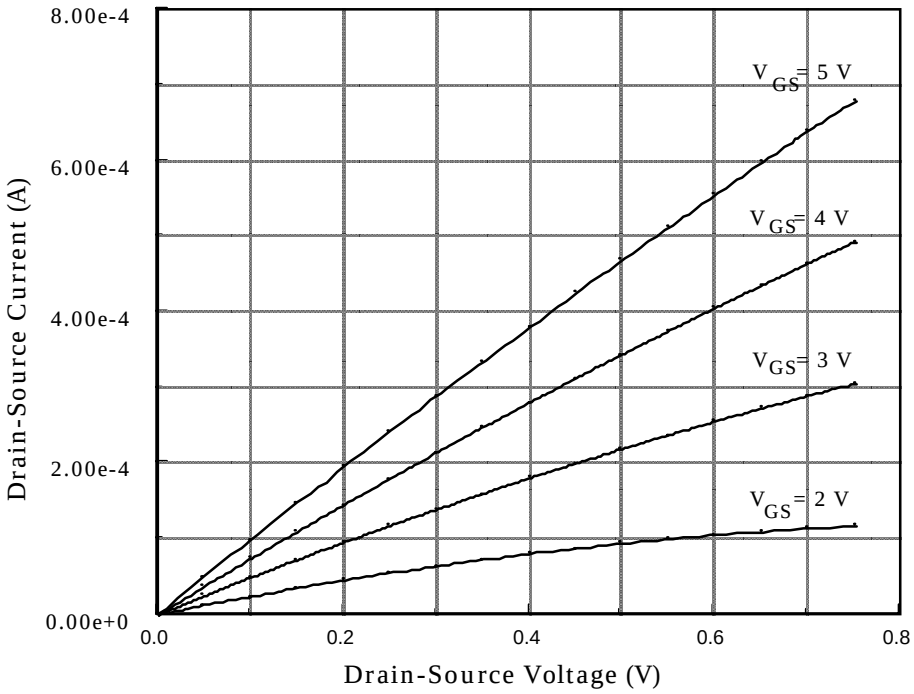


Figure 4.6 - NMOS i-v characteristics in the linear region (V_{SB} = 0)

The resistance of the FET in the linear region near the origin, called the on-resistance *Ron*, is defined as

$$R_{on} = \left\{\frac{i_{DS}}{v_{DS}}\Big|_{v_{DS}-0}\right\}^{-1}_{Q-point} = \frac{1}{K_n^{'}\frac{W}{L}(V_{GS} - V_{TN})}$$

4.4 Saturation of the *I-V characteristics*

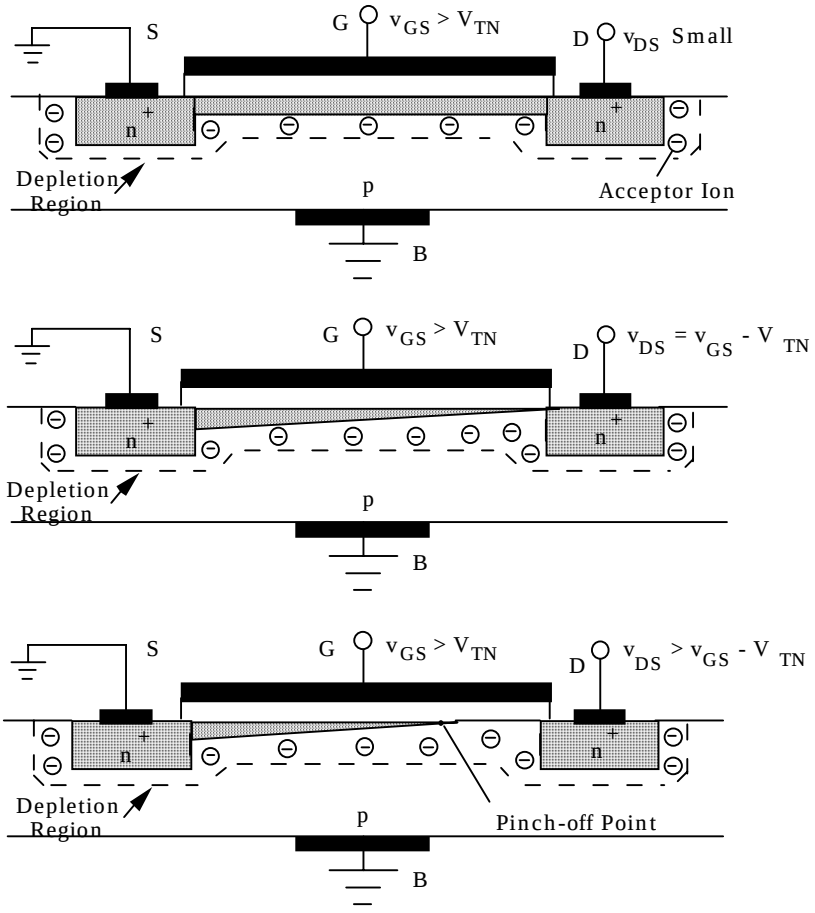


Figure 4.7 - (a) MOSFET in the linear region
(b) MOSFET with channel just pinched off at the drain
(c) Channel pinch off for $v_{DS} > v_{GS} - V_{TN}$

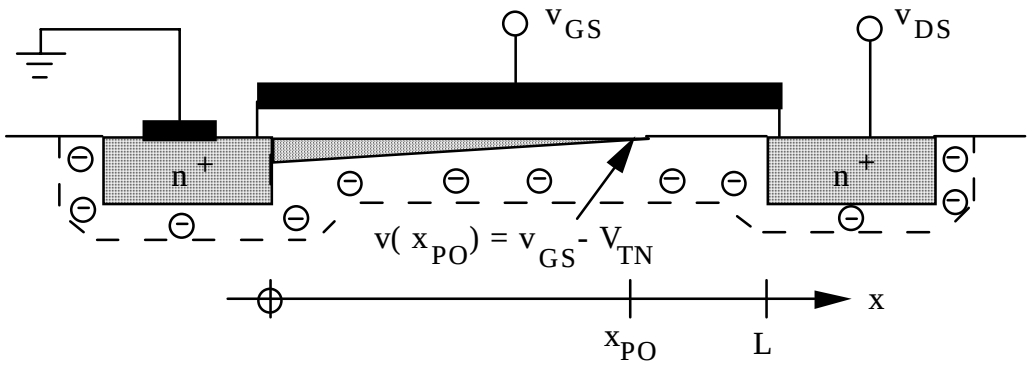


Figure 4.8 - Inversion layer in the saturation region, also known as the pinchoff region

Since the voltage across the inverted channel is constant, the drain to source current in saturation is

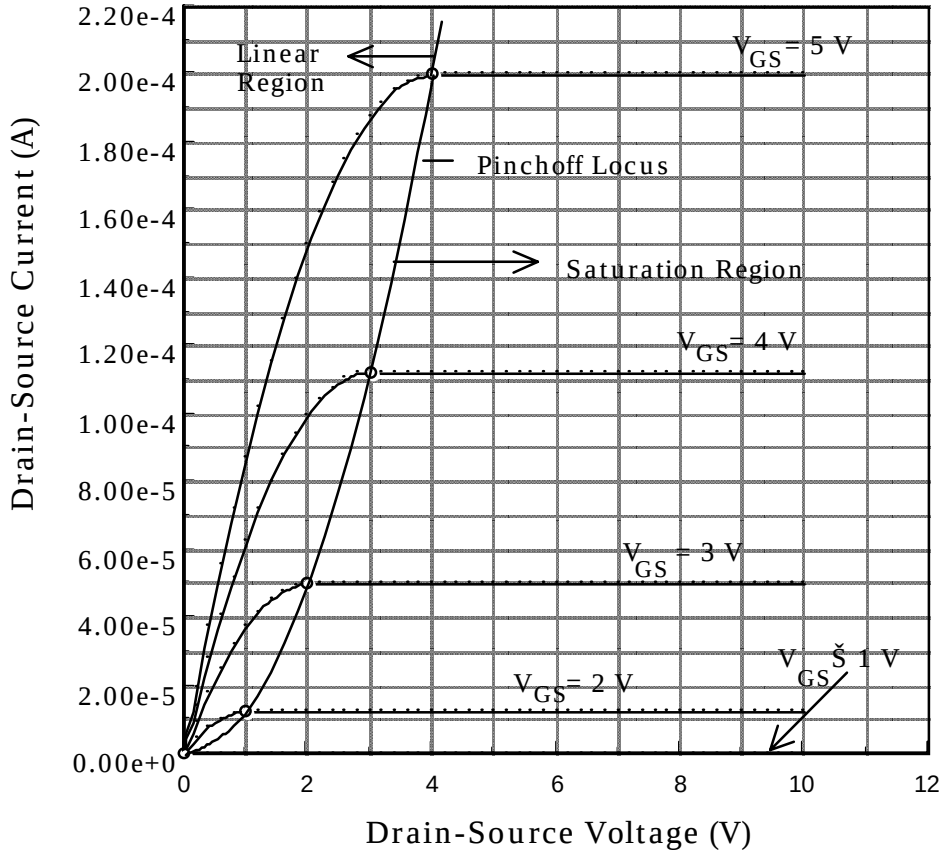


Figure 4.9 - Output characteristics for an NMOS transistor with V_{TN} = 1 V and K_n = 25 x 10^{-6} A/V^2

also constant (independent from V_{DS})

$$i_{DS} = \frac{K_N'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2 \quad \textbf{for} \quad v_{DS} \geq (v_{GS} - V_{TN}) \geq 0$$

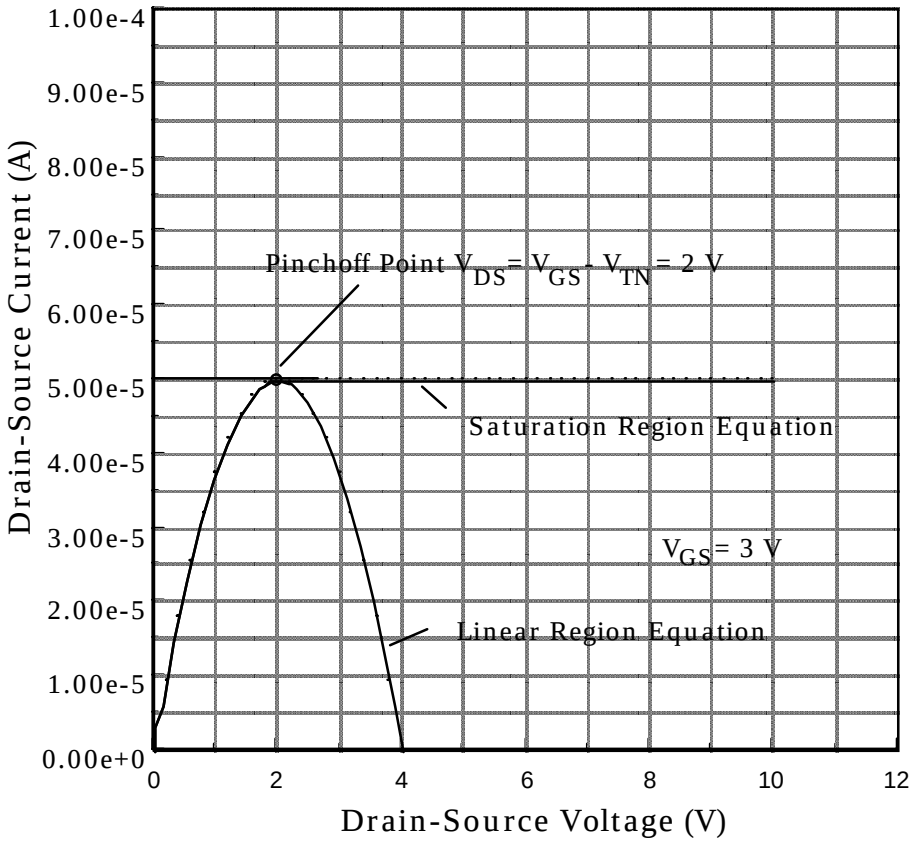


Figure 4.10 - Output characteristic showing intersection of the linear region and saturation region equations at the pinchoff point

4.6 Channel-length modulation

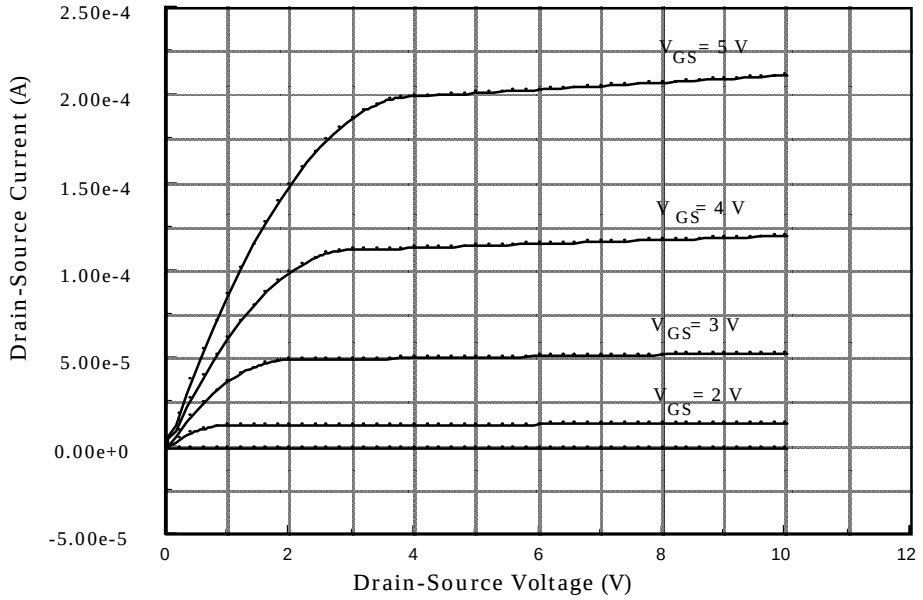


Figure 4.11 - Output characteristics including the effects of channel length modulation

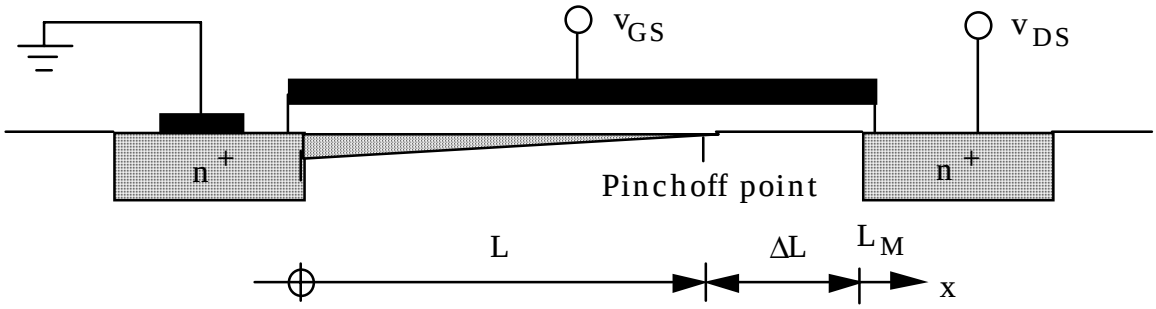


Figure 4.12 - Channel length modulation

There is an effective reduction of the channel length by increasing V_{DS} in saturation (ΔL increases).

This causes some increase in i_{DS}

$$i_{DS} = \frac{K_n'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})$$

where λ is called channel-length modulation parameter

NMOS Transistor mathematical model summary

For all regions

$$K_n = \mu_n C_{ox}'' \frac{W}{L} \qquad i_G = 0 \qquad i_B = 0$$

Cutoff region:

$$i_{DS} = 0 \quad \textbf{for} \quad v_{GS} \le V_{TN}$$

Linear region:

$$i_{DS} = K_N(v_{GS} - V_{TN} - \frac{v_{DS}}{2})v_{DS} \quad \textbf{for} \quad v_{GS} - V_{TN} \ge v_{DS} \ge 0$$

Saturation region:

$$i_{DS} = \frac{K_N}{2}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS}) \quad \textbf{for} \quad v_{DS} \ge v_{GS} - V_{TN} \ge 0$$

4.7 Transfer characteristics and the depletion-mode MOSFET

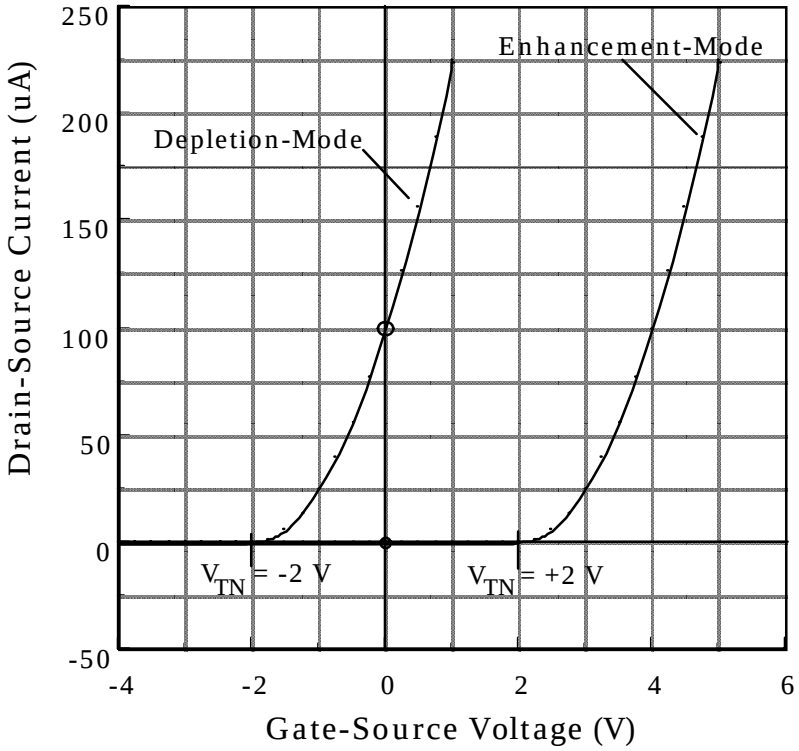


Figure 4.13 - Transfer characteristics for enhancement-mode and depletion-mode NMOS transistors

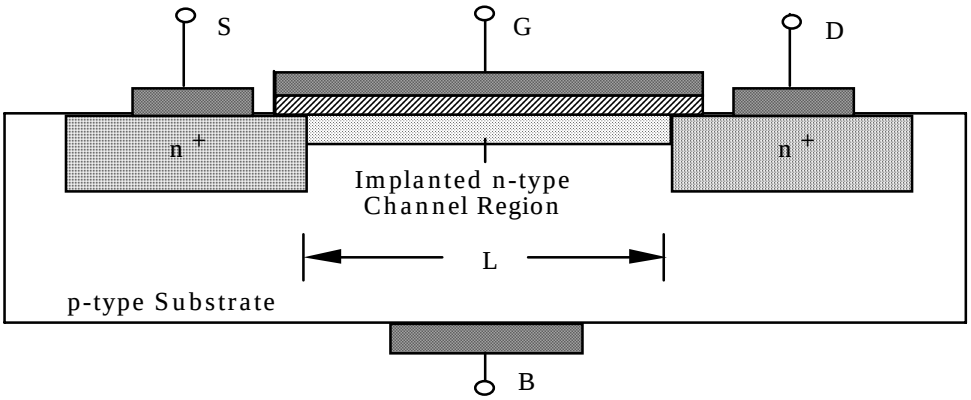


Figure 4.14 - Cross section of a depletion-mode NMOS transistor

4.8 Body effect or substrate sensitivity

$$V_{TN} = V_{TO} + \gamma(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F})$$

Where V_{TO} = **zero-substrate-bias value for** $V_{TN}(V)$

γ = **body-effect parameter** $\sqrt{V}$

$2\phi_F$ = **surface potential parameter** (V)

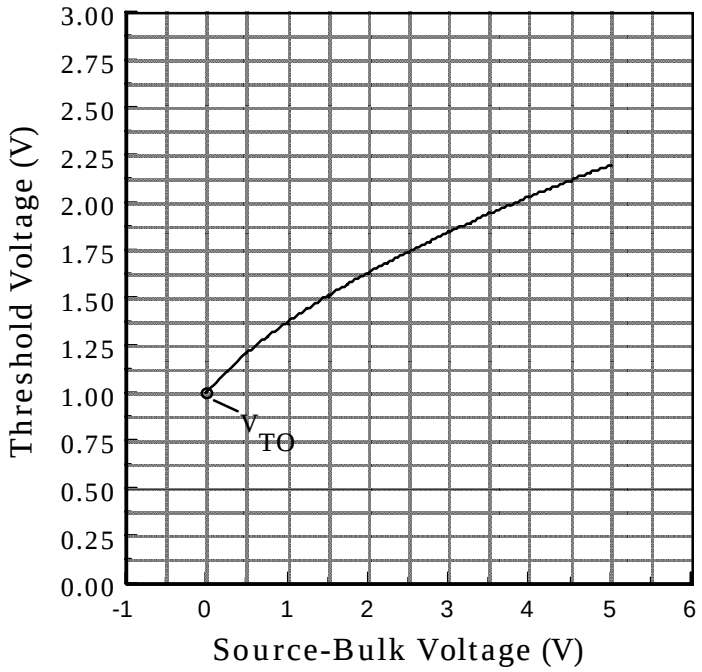


Figure 4.15 - Threshold variation with source-bulk voltage for a NMOS transistor with V_{TO} = 1 V, $2_{\phi F}$ = 0.6 V and $_{\gamma}$ = 0.75 $\sqrt{V}$.

4.9 PMOS transistors

PMOS transistor mathematical model summary

For all regions

$$K_n = \mu_n C''_{ox} \frac{W}{L} \qquad i_G = 0 \qquad i_B = 0$$

Cutoff region:

$$i_{SD} = 0 \quad \textbf{for} \quad v_{SG} \le -V_{TP} \; (v_{GS} \ge V_{TP})$$

Linear region:

$$i_{SD} = K_P \left(v_{SG} + V_{TP} - \frac{v_{SD}}{2}\right) v_{SD} \quad \textbf{for} \quad v_{SG} + V_{TP} \ge v_{SD} \ge 0$$

Saturation region:

$$i_{SD} = \frac{K_P}{2} (v_{SG} + V_{TP})^2 (1 + \lambda v_{SD}) \quad \textbf{for} \quad v_{SD} \ge v_{SG} + V_{TP} \ge 0$$

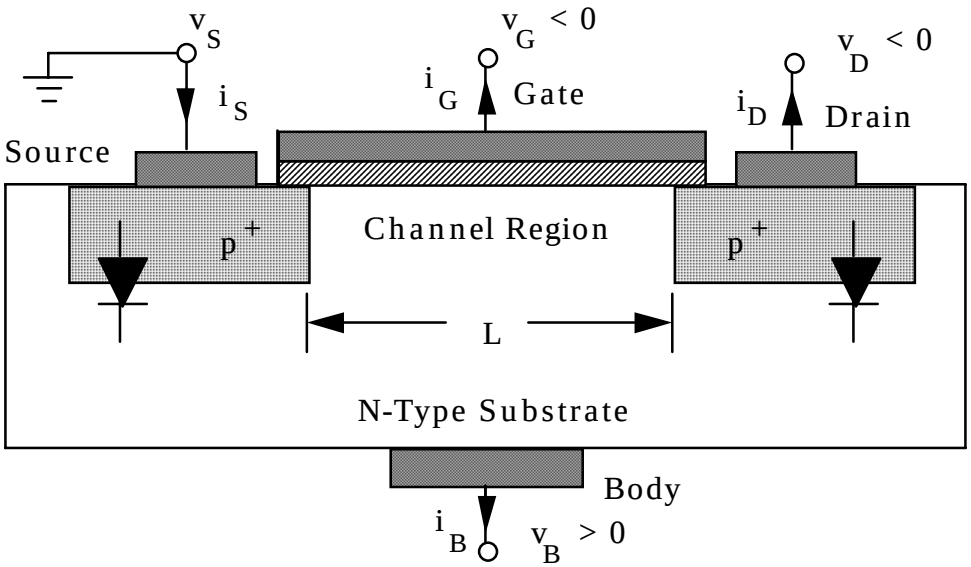


Figure 4.16 - Cross section of an enhancement-mode PMOS transistor

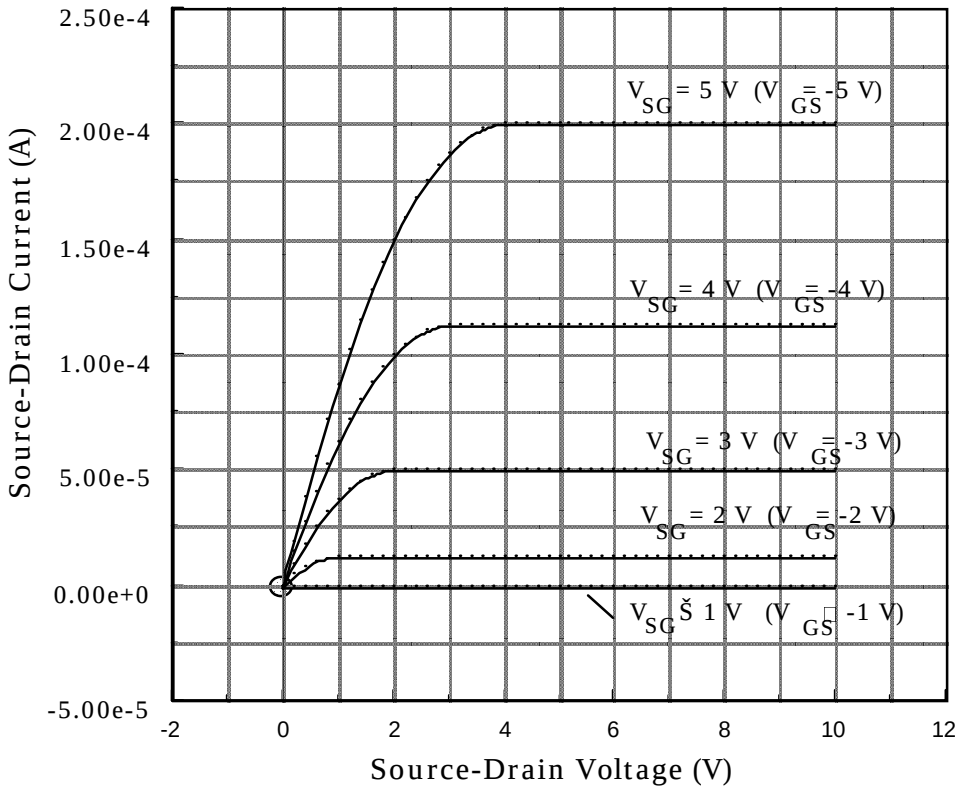
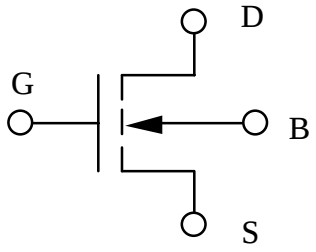


Figure 4.17 - Output characteristics for a PMOS transistor with V_{TP} = -1 V

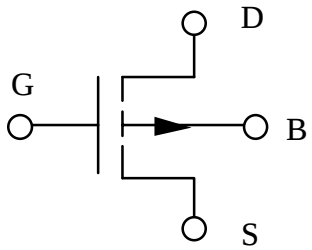
Current and voltage relationships in PMOS are like in NMOS except that their polarities are reversed.

MOSFET circuit symbols and model summary

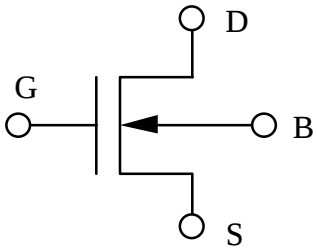
IEEE Standard MOS transistor circuit symbols



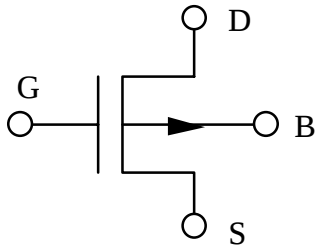
(a) NMOS enhancement-mode device



(b) PMOS enhancement-mode device

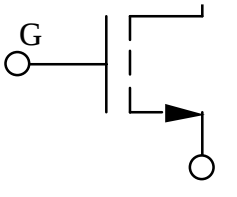


(c) NMOS depletion-mode device

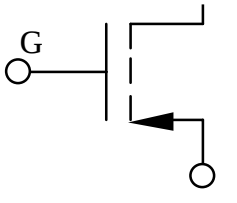


(d) PMOS depletion-mode device

Arrow points in the direction of bulk-channel diodes



(e) Three-terminal NMOS transistor



(f) Three-terminal PMOS transistor

In these symbols arrow points in the direction of the positive current

Mathematical Model Summary

NMOS Transistor model summary

For all regions $K_n = \mu_n C_{ox}'' \frac{W}{L}$ $i_G = 0$ $i_B = 0$

Cutoff region:

$$i_{DS} = 0 \quad \textbf{for} \quad v_{GS} \le V_{TN}$$

Linear region:

$$i_{DS} = K_N (v_{GS} - V_{TN} - \frac{v_{DS}}{2}) v_{DS} \quad \textbf{for} \quad v_{GS} - V_{TN} \ge v_{DS} \ge 0$$

Saturation region:

$$i_{DS} = \frac{K_N}{2} (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS}) \quad \textbf{for} \quad v_{DS} \ge v_{GS} - V_{TN} \ge 0$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma (\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F})$$

PMOS transistor mathematical model summary

For all regions

$$K_n = \mu_n C''_{ox} \frac{W}{L} \qquad i_G = 0 \qquad i_B = 0$$

Cutoff region:

$$i_{SD} = 0 \quad \textbf{for} \quad v_{SG} \le -V_{TP} \; (v_{GS} \ge V_{TP})$$

Linear region:

$$i_{SD} = K_P (v_{SG} + V_{TP} - \frac{v_{SD}}{2}) v_{SD}$$

$$\textbf{for} \quad v_{SG} + V_{TP} \ge v_{SD} \ge 0$$

Saturation region:

$$i_{SD} = \frac{K_P}{2} (v_{SG} + V_{TP})^2 (1 + \lambda v_{SD}) \quad \textbf{for} \quad v_{SD} \ge v_{SG} + V_{TP} \ge 0$$

Threshold voltage:

$$V_{TP} = V_{TO} - \gamma (\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F})$$

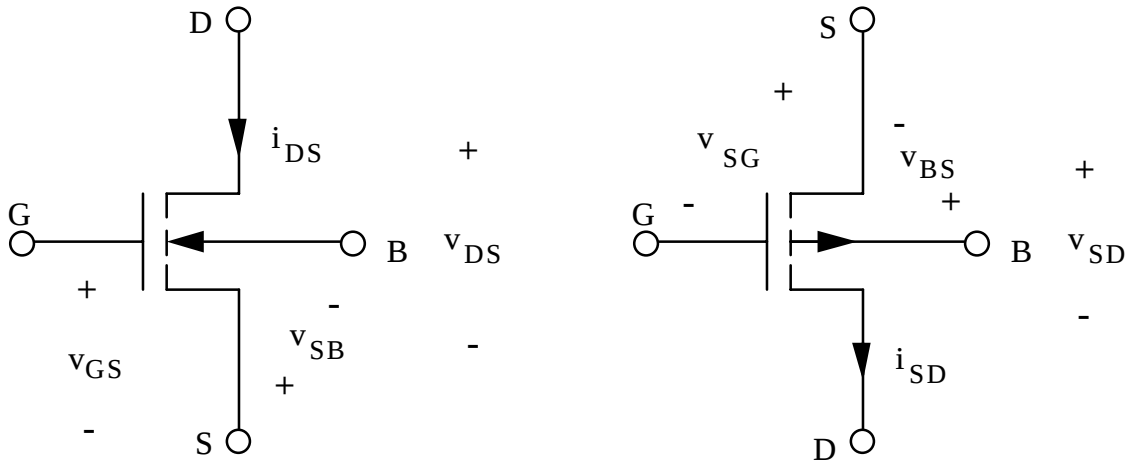


Figure 4.19 - NMOS and PMOS transistor circuit symbols

Table 4.1 - Categories of MOS Transistors

	NMOS Device	PMOS Device
Enhancement-mode	$V_{TN} > 0$	$V_{TP} < 0$
Depletion-mode	$V_{TN} <= 0$	$V_{TP} >= 0$